The P9222-R/RN is an integrated single-chip wireless power receiver IC (Rx) for up to 5W applications implementing in-band, bi-directional data communication with no additional circuitry. The device receives an AC power signal from a wireless power transmitter, such as the P9235A-RB WPC Qi BPP Wireless Transmitter IC, and converts it to a rectified output voltage, which can be used to power devices or supply the battery charger input in a wide range of wireless power applications. The receiver (Rx) integrates a high-efficiency synchronous full bridge rectifier (SFBR) and control circuits that enable bi-directional communication from and to the transmitter (Tx) for optimized power delivery.

The P9222-R/RN is highly efficient at light loads and very well-suited for low-power applications such as earbuds case charging. A unique Ping detect feature gives the user an early indication of the wireless charger connection and improves thermal performance at the end of complete battery charging. Low under-voltage lockout (UVLO) threshold allows the receiver to start up even with a weaker digital ping strength signal from a transmitter over an extended area.

The device includes over-temperature and under/over-voltage protection. The internal over-voltage clamping protects the rectifier output from rising above the overvoltage level when the receiver is quickly moved from a low-coupling position to a high-coupling position. The integrated 32-bit ARM® Cortex®-M0 processor (trademark of ARM, Ltd.) offers a high level of programmability and design parameters that can be easily configured through the I²C interface or an external EEPROM.

The P9222-R default firmware factory programmed in internal OTP is WPC 1.2.4 Qi Baseline Power Profile (BPP) compatible. The P9222-RN default factory firmware programmed in internal OTP is latest WPC 1.3 Qi Baseline Power Profile (BPP) compatible.

The P9222-R/RN is available in a RoHS ultra-small WLCSP-40 package and it is rated for a 0 to 85°C ambient operating temperature range.

Typical Applications

Wireless power solutions for mobile solutions including:

- Wireless earbuds case charging
- Wearables and fitness trackers
- Mobile devices
- Hearing aids case charging

Features

- Ultra-compact, efficient wireless power receiver for up to 5W applications
- P9222-R default firmware is WPC 1.2.4 Qi Baseline Power Profile (BPP) compatible
- P9222-RN default firmware is WPC 1.3 Qi Baseline Power Profile (BPP) compatible
- Ping detection for reduced power consumption at end of charging
- Low under-voltage lockout (UVLO) for low voltage start-up for faster connections over an extended area
- ASK and FSK modulation/demodulation for Bi-directional Communication: Rx-to-Tx and Tx-to-Rx
- Supports bi-directional data communication
- Easy configuration of design parameters through I²C interface on an external EEPROM
- Embedded 32-bit ARM® Cortex®-M0 processor
- Internal over-voltage clamping
- Low standby and operating mode power consumption
- High performance low dropout (LDO) regulator with low RDS(on) and programmable current limiting
- Supports I²C slave/master mode
- 40-WLCSP: 5 × 8 ball array, 2.28 × 3.38 mm, 0.4mm pitch

Block Diagram

Figure 1. Simplified Block Diagram

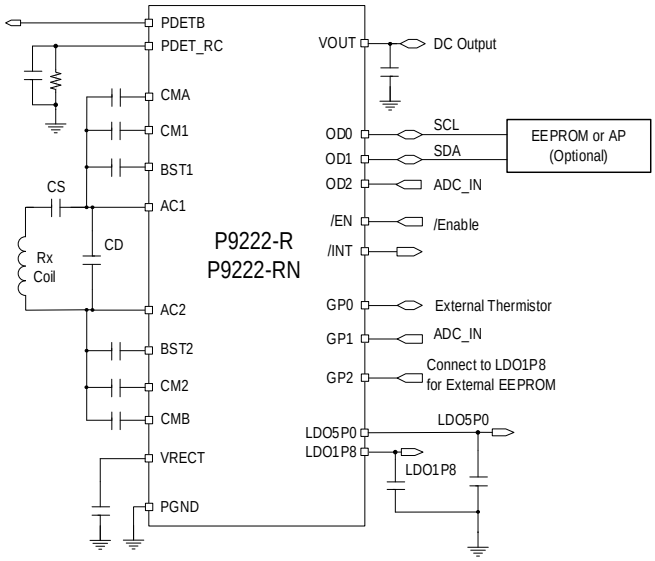
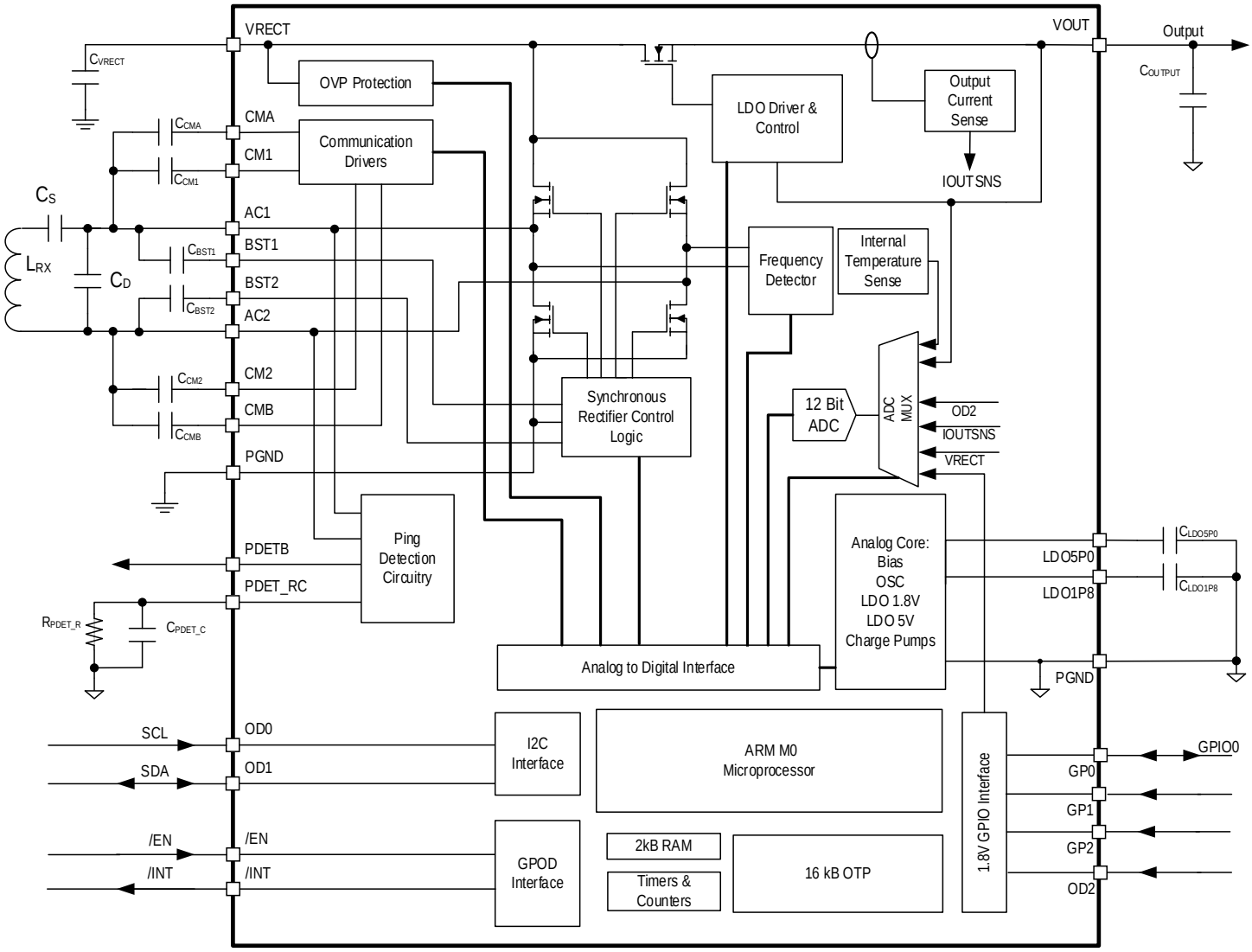


Figure 2. P9222-R/RN Block and Application Diagram



Contents

1. Pin Information 7
   1.1 Pin Assignments 7
   1.2 Pin Descriptions 8
2. Specifications 10
   2.1 Absolute Maximum Ratings 10
   2.2 Thermal Characteristics 10
   2.3 Electrical Characteristics 11
3. Description of the Wireless Power Charging System 15
4. Typical Performance Characteristics 16
5. Theory of Operation 18
   5.1 Overview 18
      5.1.1 Low-Power Ping Detection 18
      5.1.2 Rx Operation 18
   5.2 Wireless Power Control 18
   5.3 Startup 18
   5.4 Power Transfer 19
   5.5 Synchronous Rectifier 19
   5.6 Over-Voltage Protection 19
   5.7 Over-Current Protection and Thermal Shutdown 19
   5.8 External Temperature Sensing 19
   5.9 Rectifier and VRECT Level 20
   5.10 Interrupt Output 20
   5.11 Low Drop-Out (LDO) Regulators 21
   5.12 MLDO Output Enable Conditions 21
   5.13 Output Power Options 21
6. Bi-directional User Data Communication 22
   6.1 Transferring Data from the P9222-R/RN to the P9235-RB 22
   6.2 Reading Data Sent from the P9235-RB to the P9222-R/RN 25
7. WPC Mode Characteristics 27
   7.1 WPC-Compliant Power Transfer 27
   7.2 Advanced Foreign-Object Detection (FOD) in WPC Mode 27
   7.3 WPC Modulation/Communication 27
   7.4 Bit Encoding Scheme for ASK 28
   7.5 System Feedback Control 29
      7.5.1 Selection 29
      7.5.2 Ping 30
      7.5.3 Identification and Configuration 30
      7.5.4 Power Transfer 30

8. Applications Information 31
8.1 Receiver Coil 31
8.2 Series and Parallel Resonant Capacitor Selection 31
8.3 VRECT Pin 32
8.4 Enable Pin 32
8.5 Transient Voltage Suppressor Diodes (TVS) 32
8.6 GPIO Pins 33
8.6.1 OD0 Pin 33
8.6.2 OD1 Pin 33
8.6.3 OD2 Pin 33
8.6.4 GP0 Pin 33
8.6.5 GP1 Pin 33
8.6.6 GP2 Pin 34
8.7 Low-Power Ping Detection Operation 34
8.8 Configuration of P9222-R/RN Parameters 36
8.9 P9222-R/RN Internal Register Access by Application Processor 36
8.10 External EEPROM Access by P9222-R/RN 36
9. Examples of User Customizing P9222-R/RN Operating Parameters 37
9.1 LDO Output Voltage (VOUT) Configuration 37
9.1.1 VOUT Adjustment via the I2C Interface 37
9.1.2 VOUT Configuration Change Using an External EEPROM 38
9.2 Current Limit (ILIM) Configuration 38
9.3 Overvoltage (OV) Protection Configuration 39
9.4 FOD (Foreign Object Detection) 39
9.4.1 Configuring FOD Parameters 40
9.4.2 Modulation Capacitor and Interrupt Enables 41
10. I2C Function 42
11. Registers 42
12. Application Schematic 53
13. Package Outline Drawings 54
14. Marking Diagram 54
15. Ordering Information 54
16. Revision History 55

List of Figures

Figure 1. Simplified Block Diagram 1
Figure 2. P9222-R/RN Block and Application Diagram 2
Figure 3. Pin Assignments for 40-WLCSP (AZG40), 2.28 × 3.38 mm with 0.4mm Pitch – Top View 7
Figure 4. Block Diagram of WPC Compliant Wireless Power Transfer System 15

Figure 5. System Efficiency vs Output Current 16
Figure 6. VRECT vs IOUT, Vout = 5.0V 16
Figure 7. Reported Received Power (RPP) vs Iout on NOK9 Transmitter 16
Figure 8. PDIFF (PTX-PRX) vs Iout on NOK9 Transmitter 16
Figure 9. Initial Startup 17
Figure 10. Active Charging Area (Efficiency, 14 × 15 mm) 17
Figure 11. Load Transient Response 1 (Vout = 5V, Iout 0mA to 500mA) 17
Figure 12. Load Transient Response 2 (Vout = 5V, Iout 0mA to 1000mA) 17
Figure 13. Ping Detect Timing 17
Figure 14. AC Modulation (COM1) 17
Figure 15. RTH1 and R21 Schematic Location 20
Figure 16. RTH1 and R21 PCB Location 20
Figure 17. Timing Diagram for a User Data Transfer from the P9222-R/RN to the P9235-RB 23
Figure 18. Typical P9222-R/RN to P9235-RB Data Transfer using the P9235A-RB-EVK Evaluation Kit 23
Figure 19. State Diagram for User Data Transmission from the P9222-R/RN to the P9235-RB 24
Figure 20. State Diagram for Reading User Data Received from the P9235-RB 26
Figure 21. Rx Modulation Components 27
Figure 22. Communication Packet Structure 28
Figure 23. WPC Packet Example with Reference Clock Shown 28
Figure 24. Byte Encoding Scheme 28
Figure 25. WPC System Feedback Control BPP Mode 29
Figure 26. Dual Resonant Circuits with Receiver Coil 31
Figure 27. P9222-R/RN Recommended Enable Default State Configurations 32
Figure 28. GP0 Pin External Connection to Thermistor Configuration 33
Figure 29. GP2 Pin External Connections for External EEPROM Selection 34
Figure 30. Ping Detection – Typical Application Schematic Components and Connections 34
Figure 31. P9222-R/RN Ping Detect Waveforms 35
Figure 32. Writing to the Vout_Set Register using P9222-R/RN Windows GUI 37
Figure 33. Changing the Default VOUT Value using the P9222-R/RN Windows GUI 38
Figure 34. Changing the Default FOD Registers using the P9222-R/RN Windows GUI 40
Figure 35. Modulation and INT Settings Tab 41
Figure 36. P9222-R/RN Application Schematic 53

List of Tables

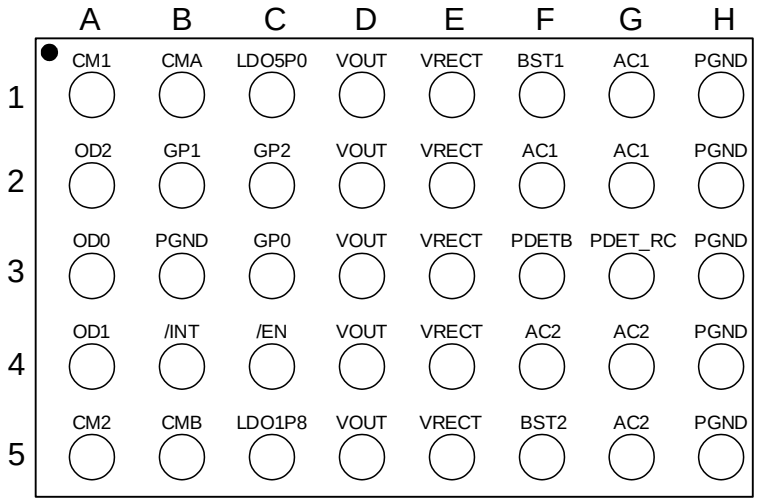
Table 1. Pin Descriptions 8
Table 2. Absolute Maximum Ratings 10
Table 3. Thermal Characteristics for 40-WLCSP Package 10
Table 4. ESD Information 11
Table 5. Electrical Characteristics 11
Table 6. Registers Used for Data Transmission from P9222-R/RN to P9235-RB 22

Table 7. Registers Used for Reading User Data from the P9235-RB....25
Table 8. Recommended Coil Manufacturer....31
Table 9. Recommended RC Values for PDET_RC Components Based on Capacitance and Ping Interval....35
Table 10. Recommended Maximum Estimated Power Loss....39
Table 11. Chip Part Number ID Register, Chip_ID_L (0x00), Chip_ID_H (0x01)....42
Table 12. Chip Revision Register, Chip_Rev (0x02)....42
Table 13. Status Registers, Status_L (0x34), Status_H (0x35)....43
Table 14. Interrupt Registers, INT_L (0x36), INT_H (0x37)[a]....43
Table 15. Interrupt Enable Registers, INT_Enable_L (0x38), INT_Enable_H (0x39)....44
Table 16. Interrupt Clear Registers, INT_Clear_L (0x3A), INT_Clear_H (0x3B)....44
Table 17. Vout Set Register, Vout_Set (0x3C)....45
Table 18. ILIM Set Register, ILIM_Set (0x3D)....45
Table 19. Battery Charge Status Register, CHG_Status (0x3E)[a]....45
Table 20. End of Power Transfer Register, EPT (0x3F)[a]....46
Table 21. Vrect ADC Value Registers, ADC_Vrect_L (0x40), ADC_Vrect_H (0x41)....46
Table 22. Vout ADC Value Registers, ADC_Vout_L (0x42), ADC_Vout_H (0x43)....46
Table 23. Iout Value Registers, Iout_L (0x44), Iout_H (0x45)....46
Table 24. Operating Frequency Registers, Op_Freq_L (0x48), Op_Freq_H (0x49) (RX Only)....46
Table 25. System Operating Mode Register, Sys_Op_Mode (0x4C)....47
Table 26. (AP to P9222-R/RN) Command Register, COM (0x4E)....47
Table 27. Outgoing Packet Header Register (0x50, 8-bit)....48
Table 28. Outgoing Packet Data Registers (0x51-0x57, 8-bit)....48
Table 29. Incoming Packet Header Register (0x50, 8-bit)....48
Table 30. Incoming Packet Data Registers (0x59-0x5F, 8-bit)....48
Table 31. Die Temperature ADC Value Registers, ADC_Die_Temp_L (0x66), ADC_Die_Temp_H (0x67)....49
Table 32. Overvoltage Protection Set Register (0xB3, 8-bit)....49
Table 33. ASK Modulation Depth Register (0xB2, 16-bit)....49
Table 34. Foreign Object Detection Registers, FOD (0x70-0x7E)[a]....50
Table 35. ADC Result Register (0xD4, 16-bit, OD2 in Default Config)....50
Table 36. ADC Result Register (0xD6, 16-bit, GP1 in Default Config)....51
Table 37. ADC Result Register (0xD8, 16-bit, GP2 in Default Config)....51
Table 38. ADC Result Register (0xDA, 16-bit, Die Temperature in Default Config)....51
Table 39. External Thermistor Voltage on GP0 (0xB0, 16-bit)....51
Table 40. VRECT Target Register (0x90, 16-bit)....51
Table 41. VRECT Knee Register (0x92, 8-bit)....52
Table 42. VRECT Correction Factor Register (0x93, 8-bit)....52
Table 43. VRECT Maximum Correction Register (0x94, 16-bit)....52
Table 44. VRECT Minimum Correction Register (0x96, 16-bit)....52

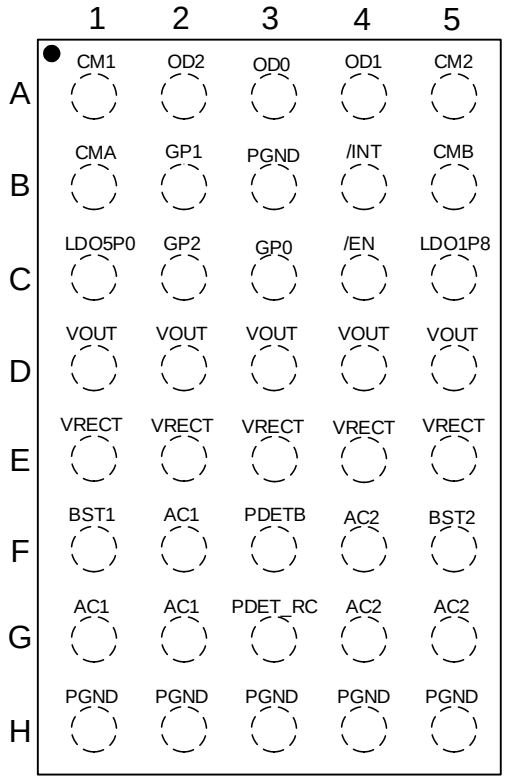
1. Pin Information

1.1 Pin Assignments

Figure 3. Pin Assignments for 40-WLCSP (AZG40), 2.28 × 3.38 mm with 0.4mm Pitch – Top View



P9222-R/ P9222-RN CSP (Ball View)



P9222-R/ P9222-RN CSP (Top View)

1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
A1	CM1	Output	High-voltage, open-drain output from the modulation FETs. Connect a 47nF capacitor from AC1 to CM1.
A2	OD2	Input/Output	Open-drain GPIO. This pin is connected to the internal ADC and can measure voltages smaller than 1.2V. This pin can be left floating if not used.
A3	OD0/SCL	Input/Output	Open-drain GPIO. This pin supports an input of up to 5V, and is used for the I2C SCL connection. Connect this pin via a pull-up resistor to the system I/O supply. This pin can be left floating if not used.
A4	OD1/SDA	Input/Output	Open-drain GPIO. This pin supports an input of up to 5V, and is used for the I2C SDA connection. Connect this pin via a pull-up resistor to the system I/O supply. This pin can be left floating if not used.
A5	CM2	Output	High-voltage, open-drain output from the modulation FETs. Connect a 47nF capacitor from AC2 to CM2.
B1	CMA	Output	High-voltage, open-drain output from the modulation FETs. By default, CMA capacitor is not used for communication. This pin can be left floating if not used.
B2	GP1/ADC IN	Input/Output	GPIO1. Pin is connected to internal ADC and can measure system voltage smaller than 1.8V. During startup this pin is set as a high-impedance. This pin can be left floating if not used.
B3, H1-H5	PGND	GND	Power and logic ground.
B4	/INT	Output	Interrupt output pin. Connect this pin to the application processor (AP) I/O voltage rail using an external pull-up resistor. The P9222-R/RN drives this pin LOW to notify the AP host of status changes.
B5	CMB	Output	High-voltage, open-drain modulation FETs. By default, CMB capacitor is not used for communication. This pin can be left floating if not used.
C1	LDO5P0	Output	Internal 5V LDO for chip power only. Connect a 1µF and 0.1µF capacitor to ground.
C2	GP2	Input	GPIO2. If this pin is pulled high to the internal 1.8V LDO (LDO1P8) using a 10K resistor, the P9222-R/RN becomes an I2C master during startup to load 100 bytes of user configuration from external EEPROM. If this pin is pulled to ground, the P9222-R/RN loads the default configuration from the internal OTP.
C3	GP0/ Thermistor	Input/Output	GPIO0. This pin can be used to measure coil temperature. The P9222-R/RN interrupts the processor when the coil voltage goes below 0.6V. During the startup this pin is set as a high-impedance. Pull this pin to 1.8V with a resistor if not used.
C4	/EN	Input	Active-LOW enable pin. To enable the P9222-R/RN, pull this pin to GND. To disable the P9222-R/RN, pull this pin High.
C5	LDO1P8	Output	Internal 1.8V LDO output for logic power. Connect a 1µF and 0.1µF capacitor to ground.
D1-D5	VOUT	Output	Main LDO output pin. Connect at least a 1×10µF capacitor from this pin to ground. It is not recommended to directly connect the USB charging port or other voltage sources to these pins. Back-to-back isolation FETs are recommended.
E1-E5	VRECT	Input/Output	Filter capacitor for the internal rectifier. Capacitance requirements: Connect 2×10µF and 1×0.1µF capacitors in parallel from this pin to ground.
F1	BST1	Output	Bootstrap capacitor for driving the high side NFETs of the internal rectifier. Connect a 15nF capacitor from AC1 to BST1.

Pin Number	Name	Type	Description
F2, G1, G2	AC1	Input	AC power input 1. Connect AC1 to the C_S capacitors and C_S to the Rx coil. Connect the C_D capacitor from AC1 to AC2 (see Figure 2 and the application schematic in Figure 36). Due to symmetry, the AC1 and AC2 connections are interchangeable.
F3	PDETB	Output	Open-drain, active-LOW. This pin is an output for indicating ping events are being received by the Rx. Connect this pin to the application processor (AP) I/O voltage rail using an external pull-up resistor.
F4, G4, G5	AC2	Input	AC power input 2. Connect this pin to the Rx coil and the C_D capacitor (see Figure 2) Due to symmetry, the AC1 and AC2 connections are interchangeable.)
F5	BST2	Output	Bootstrap capacitor for driving the high-side NFETs of the internal rectifier. Connect a 15nF capacitor from AC2 to BST2.
G3	PDET_RC	Input	Ping-detect input pin for determining when PDETB will be de-asserted. This pin is used to notify the AP if the Rx device is removed from the power transfer interface. Connect an RC time-delay circuit designed to hold the voltage on this pin above $V_{PDET_RC_IL}$ between each Tx ping after power transfer is completed (EOC).

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P9222-R/RN at the absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Conditions	Minimum[a]	Maximum[a]	Unit
VRECT, AC1, AC2, CMA, CMB, CM1, CM2		-0.3	20	V
PDETB, PDET_RC, LDO5P0, OD[2:0]		-0.3	6	V
LDO1P8, GP[2:0], /INT, /EN		-0.3	2	V
BST1		AC1 – 0.3	AC1 + 6	V
BST2		AC2 – 0.3	AC2 + 6	V
VOUT		-0.3	13	V
PGND		-0.3	0.3	V
Maximum RMS Current from CMA, CMB, CM1, CM2			500	mA
Maximum RMS Current from AC1, AC2			2	A

[a] All voltages are referenced to ground unless otherwise noted.

2.2 Thermal Characteristics

Table 3. Thermal Characteristics for 40-WLCSP Package

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Ambient[a][b][c][d]	47	°C/W
θ_{JC}	Thermal Resistance Junction to Case[b][c][d]	0.202	°C/W
θ_{JB}	Thermal Resistance Junction to Board[b][c][d]	4.36	°C/W
T_J	Operating Junction Temperature[a][b]	-40 to +125	°C
T_A	Operating Ambient Temperature[a][b]	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} – T_A / \theta_{JA}$ where T_J is the junction temperature and $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51 standard four-layer board with dimensions 3” × 4.5” in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, airflow, altitude, and other unlisted variables.

[d] For the 40-WLCSP (AZG40) package, connecting the six thermal balls to the internal/external ground planes from the top to bottom sides of the PCB is recommended for improving the overall thermal performance.

Table 4. ESD Information

Test Model	Pins	Ratings	Unit
Human Body Model (HBM)	All pins.	±2000	V
Charged-Device Model (CDM)	All pins.	±500	V

2.3 Electrical Characteristics

Table 5. Electrical Characteristics

See important notes at the end of the table. V_{VRECT} = 5.5V[a], $\overline{EN}$ = 0V, and C_{OUT} = 10µF unless otherwise noted. T_J = -10°C to 125°C. Typical values are at 25°C.

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
V_{RECT} and Under-Voltage Lock-Out						
V_{RECT}	V_{RECT} Operating Voltage[a][b]		3.5	5.5	12.5	V
V_{UVLO_RISING}	UVLO Rising	Rising voltage on VRECT pin		2.5	2.8	V
$V_{UVLO_FALLING}$	UVLO Falling	Falling voltage on VRECT pin	2.1	2.3		V
V_{UVLO_HYS}	UVLO Hysteresis	Falling hysteresis voltage on VRECT pin	100	200	300	mV
Over-Voltage Protection						
V_{OVP}	Over-Voltage Protection	OVP rising voltage on VRECT pin (default, programmable)	14	15	16	V
$V_{OVP\text{-}HYS}$	Over-Voltage Hysteresis			1		V
$V_{PRE\text{-}CLAMP}$	Pre-Clamp Over-Voltage Protection	Pre-clamp, rising voltage on the VRECT pin (Default, programmable), V_{MLDO} = 5V		12		V
$I_{PRE_CLAMP_RNG}$	Pre-Clamp Current Range[c]	Programmable	0		137	mA
$I_{PRE_CLAMP_STEP}$	Step Size			7		mA
I_{PRE_CLAMP}	Set Point	V_{RECT} = 10V, $I_{PRE_CLAMP_SET_POINT}$ = 109mA		110		mA
Quiescent Current						
$I_{RECT\text{-}IDDQ}$	I_{RECT} Quiescent Current[c]	No external load on VRECT, LDO5P0, and LDO1P8 pins; rectifier not switching; firmware loaded		8		mA
$I_{RECT\text{-}DIS}$	I_{RECT} Disable Current	No external load on VRECT, LDO5P0, LDO1P8; /EN = 1.8V; firmware loaded; rectifier not switching		2		mA
Main Low-Drop-Out (MLDO) Regulator (VOUT)						
$I_{MLDO_LMT_ACC}$	Current Limit Accuracy	Current Limit = 0.5A	-3		3	%
$I_{MLDO_LMT_RNG}$	Current Limit Range	Programmable	0.35		1.5	A

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
$I_{MLDO_LMT_STEP}$	Current Limit LSB	Programmable step		50		mA
V_{MLDO}	Regulated VOUT	Programmable; V_{VRECT} = 5.5V ,IOUT = 1A	4.8	5	5.2	V
V_{MLDO_STEP}	Output Voltage Step Size[c]			25		mV
V_{MLDO_ACC}	Output Voltage Accuracy	VOUT = 5V; IOUT = 0.5A	-2		2	%
R_{DSON_MLDO}	Main LDO			80		mΩ
V_{MLDO_DROP}	LDO Drop-Out Voltage	IOUT = 0.5A		37.5		mV
V_{MLDO_LNR}	Line Regulation	VRECT = 5.5V to 8V; IOUT = 100mA	-0.2		0.2	%
V_{MLDO_PSRR}	VOUT Power Supply Rejection Ratio[c]	VOUT = 5V; IOUT = 0.5 A; 1kHz 120mVpp signal summed with VRECT DC level.		80		dB
$MLDO_{LINETRANS}$	Line Transient[c]	VRECT = 5.5V to 8V; IOUT = 100mA, Slew Rate = 1V / 10µs		3.5		mV/V
V_{MLDO_LDR}	Load Regulation	IOUT = 0 A to 0.5 A; VOUT = 5V	-0.5		0.5	%
$MLDO_{LOADSTEP}$	Load Transient Rising[c]	VOUT = 5V; IOUT = 0 to 500mA, Slew rate = 1A/1µs		160		mV/A
t_{MLDO_SS}	MLDO Start-up Rise Time[c]	Output capacitance = 10µF; no external load (10% to 90%)		150		µs
LDO5P0 (For internal use only; LDO5P0 VIN = VRECT)						
V_{LDO5P0}	LDO5P0 Output	Output capacitance = 1µF, external load=10mA	4.5	5	5.5	V
t_{LDO5P0_SS}	LDO5P0 Start-up Rise Time[c]	Output capacitance = 1µF; no external load (10% to 90%)		160		µs
LDO1P8 (For internal use only; LDO1P8 VIN = LDO5P0)						
V_{LDO1P8}	LDO1P8 Output[d]	Output capacitance = 1µF, external load = 10mA	1.62	1.8	1.98	V
t_{LDO1P8_SS}	LDO1P8 Start-up Rise Time[c]	Output capacitance = 1µF; no external load (10% to 90%)		7		µs
Synchronous Full Bridge Rectifier						
R_{ON_HS}	High Side R_{DS_ON}			52		mΩ
R_{ON_LS}	Low Side R_{DS_ON}			52		mΩ
$R_{DSON_CMA/CMB}$	Communication A/B			1		Ω
$R_{DSON_CM1/CM2}$	Communication 1/2			1		Ω
VF_RECT	Rectifier Body Diode	Forward biased voltage; 100mA		0.65		V
$RECT_{FREQ_IN}$	Rectifier Input Operating Frequency Range[c]		100		300	kHz

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
Analog-to-Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
Channel	Number of Channels			8		#
$V_{IN,FS}$	Full Scale Input Voltage[e]			2.1		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown[f]	Threshold rising		140		°C
		Threshold falling		120		°C
Clock						
f_{CLOCK_60}	Clock Frequency		54	60	66	MHz
General Purpose Push-Pull Inputs/Outputs (GP0, GP1, /EN)						
V_{IH_GP}	Input High Level		1.4			V
V_{IL_GP}	Input Low Level				0.5	V
I_{LKG_GP}	Input Leakage Current	0V and 1.8V	-1		+1	µA
V_{OH_GP}	Output Logic High	I_{OH} = 4mA, 8mA total	1.44			V
V_{OL_GP}	Output Logic Low	I_{OL} = 8mA			0.36	V
SCL, SDA (OD0, OD1) and General Purpose Open Drain Inputs/Outputs (OD2, OD3, /INT)						
V_{IH_OD}	Input High Level[g]		1.4			V
V_{IL_OD}	Input Low Level[g]				0.7	V
I_{LKG_OD}	Input Leakage Current	V = 0V and 5V (1.8V for /INT)	-1		+1	µA
V_{OL_OD}	Output Logic Low	I_{OL} = 8mA			0.36	V
Ping Detection						
$V_{PDET_RC_IH}$	Input High Level	PDET_RC pin ≥ VPDET_RC_IH for PDET_B pin to be pulled-low.	2.2			V
$V_{PDET_RC_IL}$	Input Low Level	PDET_RC pin ≤ VPDET_RC_IL for PDET_B pin to be pulled-high (external pull-up required).			0.5	V
$I_{PDET_RC_LKG}$	PDET_RC Leakage	V_{VRECT} = 0V and V_{VRECT} = 5.5V	-1		+1	µA
V_{PDETB_OL}	Output Logic Low	I_{OL} = 1mA			0.36	V
SCL, SDA (I2C Interface OD0, OD1)						
f_{SCL}	Clock Frequency				400	kHz
t_{HD_STA}	Hold Time (Repeated) for START Condition		0.6			µs
t_{HD_DAT}	Data Hold Time		0			ns

Symbol	Description	Conditions	Minimum	Typical	Maximum	Unit
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
t_{SU_STA}	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
V_{IL_I2C}	Input Low Level				0.7	V
V_{IH_I2C}	Input High Level		1.4			V
I_{LKG_I2C}	Input Leakage Current	V = 0V and 5V	-1		+1	µA
V_{OL_I2C}	Output Logic Low	I_{OL}= 8mA			0.36	V

[a] V_{RECT} can be as high as 18V but the device “Electrical Characteristics” table limits are not guaranteed under this condition.

[b] Full power transfer might not occur at the minimum VRECT operating specification.

[c] Not 100% production tested. Guaranteed by design.

[d] For internal biasing only; can be used for weak pull-ups or EEPROM power (not to exceed 10mA total).

[e] Any open-drain GPIO (OD2) that is connected to the ADC should remain below 2.1V to prevent saturation of the ADC.

[f] The internal temperature is monitored, and the P9222-R/RN is temporarily deactivated if the temperature exceeds the thermal shutdown limit of 140°C typically. The P9222-R/RN is reactivated when the temperature falls below the thermal shutdown hysteresis (20°C typically).

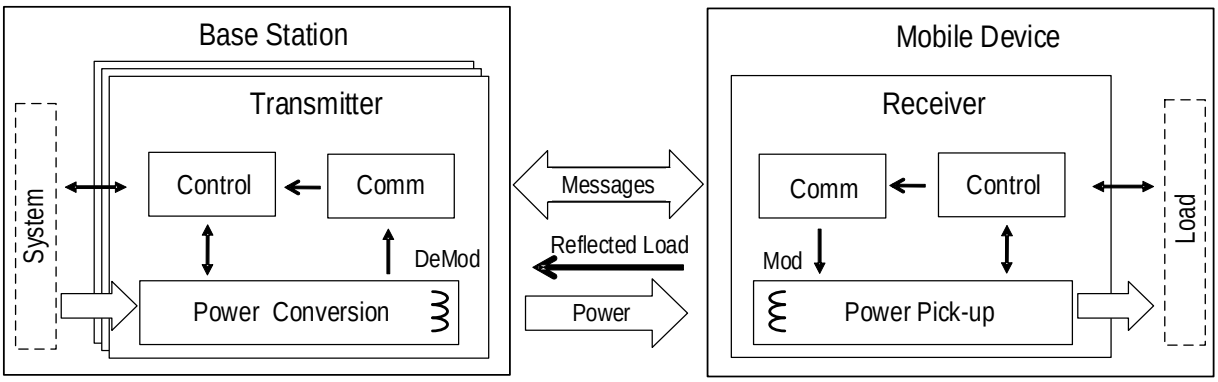
[g] The pull-up voltage level can be connected to LDO5P0 (5V) or LDO1P8 (1.8V).

3. Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitter coils that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair (magnetic induction), or over a loosely-coupled inductor pair (magnetic resonance) to a receiver in a mobile device. A WPC (see Figure 4) uses near-field magnetic induction between coils and can be a free-positioning or magnetically-guided type of system.

In WPC Inductive systems, the amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The bit rate for the Rx-to-Tx communication link is 2kbps for WPC receivers. It is modulated on top of the power link that exists.

Figure 4. Block Diagram of WPC Compliant Wireless Power Transfer System



Note: For the more current information, see the *WPC Specification* at http://www.wirelesspowerconsortium.com/.

4. Typical Performance Characteristics

The following performance characteristics were taken using a P9235-RB-EVK, with WPC A11a coil and P9222-R/RN EVK with MQQRR303008S8R2 coil with default configuration in at T_A = 25°C unless otherwise noted.

Figure 5. System Efficiency vs Output Current

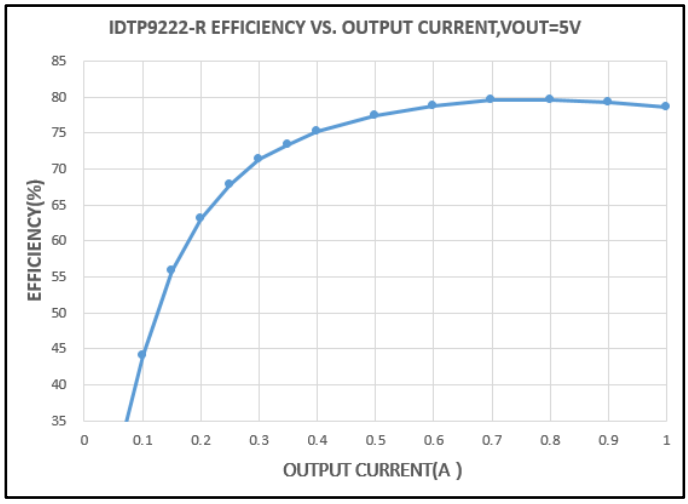


Figure 6. VRECT vs IOUT, Vout = 5.0V

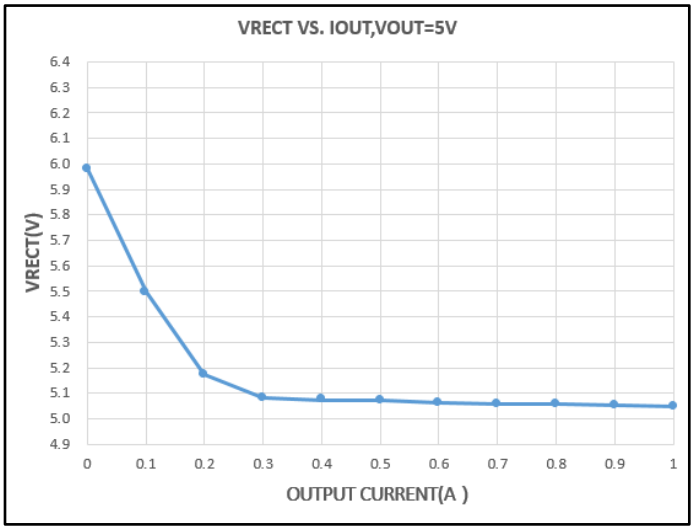


Figure 7. Reported Received Power (RPP) vs Iout on NOK9 Transmitter

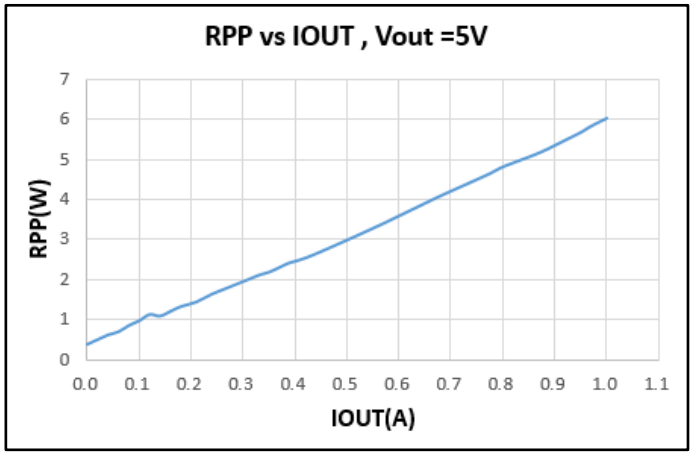


Figure 8. P_{DIFF} (P_{TX}-P_{RX}) vs Iout on NOK9 Transmitter

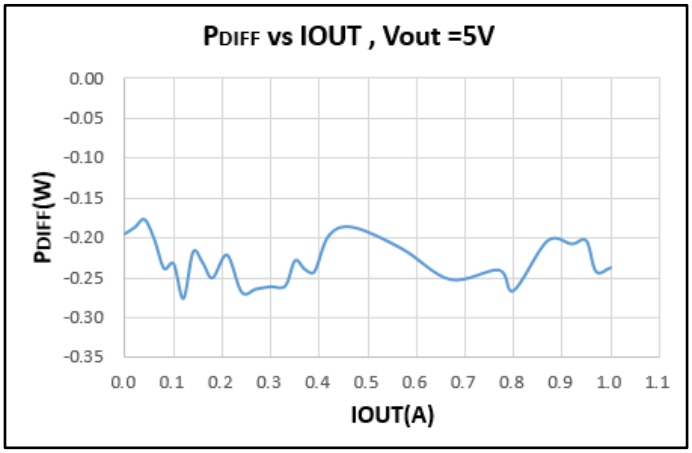


Figure 9. Initial Startup

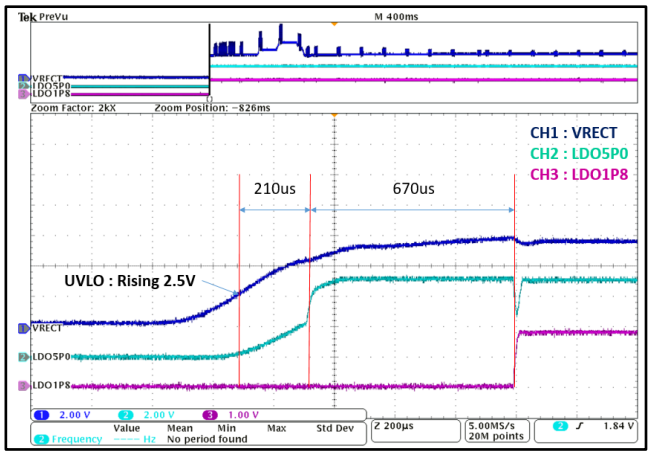


Figure 10. Active Charging Area (Efficiency, 14 × 15 mm)

	9	8	7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	9
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	77	77	77	77	77	76	0	0	0	0	0	0
6	0	0	0	0	0	77	77	78	78	78	78	78	77	77	0	0	0	0	0
5	0	0	0	0	77	77	78	78	79	79	79	79	78	78	77	0	0	0	0
4	0	0	0	77	77	78	79	79	79	79	79	79	79	78	78	77	0	0	0
3	0	0	76	77	78	79	79	79	79	80	79	80	79	79	78	77	76	0	0
2	0	0	77	78	78	79	79	80	80	80	80	80	80	79	79	78	77	0	0
1	0	0	77	78	79	79	80	80	80	80	80	80	80	79	79	78	77	0	0
0	0	0	77	78	79	79	80	80	80	80	80	80	80	80	79	78	77	0	0
1	0	0	77	78	79	79	80	80	80	80	80	80	80	79	79	78	77	0	0
2	0	0	77	78	79	79	80	80	80	80	80	80	80	79	79	78	77	0	0
3	0	0	76	78	78	79	79	80	80	80	80	80	80	79	79	78	77	0	0
4	0	0	0	77	78	79	79	79	79	80	80	80	79	79	78	77	0	0	0
5	0	0	0	76	77	78	79	79	79	79	79	79	79	79	78	78	77	0	0
6	0	0	0	0	77	77	78	78	79	79	79	78	78	78	0	0	0	0	0
7	0	0	0	0	0	0	77	78	78	78	78	78	77	77	0	0	0	0	0
8	0	0	0	0	0	0	0	0	77	77	77	76	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 11. Load Transient Response 1 (Vout = 5V, Iout 0mA to 500mA)

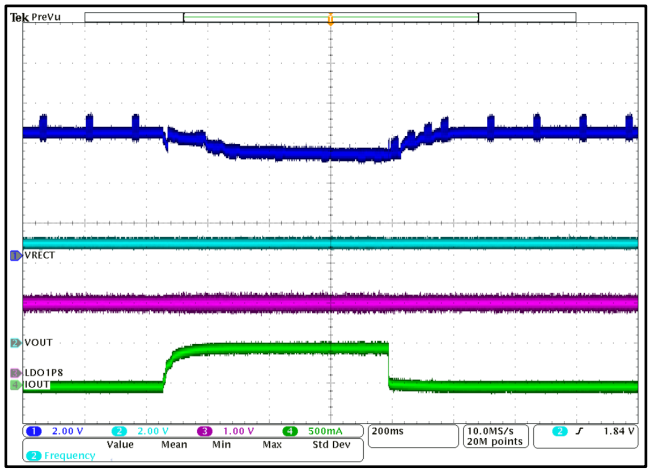


Figure 12. Load Transient Response 2 (Vout = 5V, Iout 0mA to 1000mA)

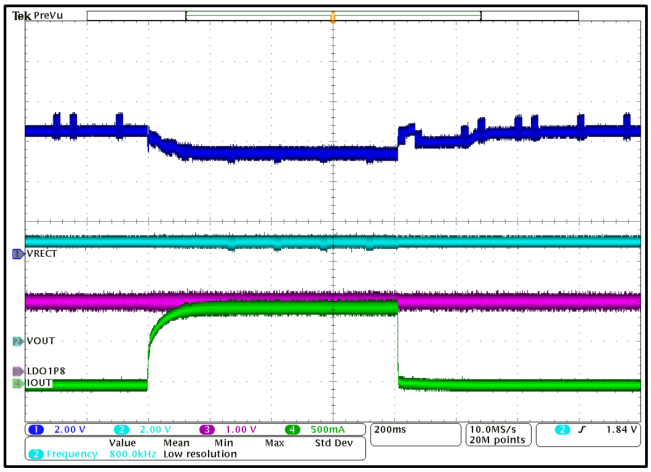


Figure 13. Ping Detect Timing

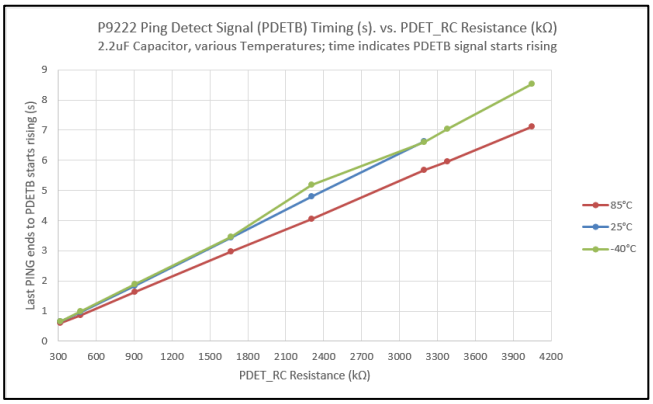
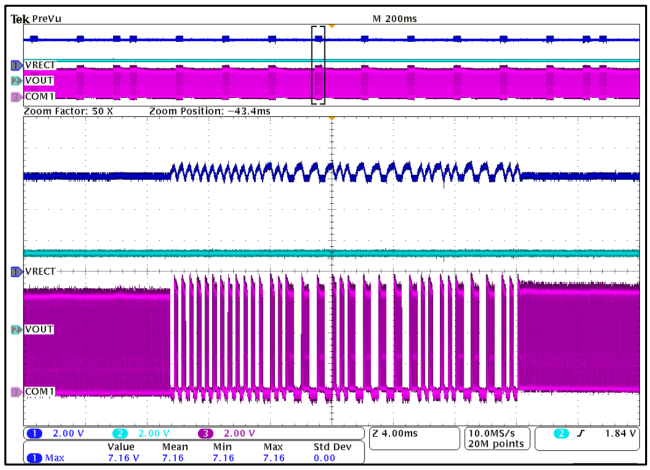


Figure 14. AC Modulation (COM1)



5. Theory of Operation

The P9222-R/RN is a highly-integrated wireless power receiver for mobile or stationary devices. The device can receive and provide up to 5W to its output when powered wirelessly using near-field magnetic induction. The device is optimized for efficient power transfer in low-power wearable applications.

5.1 Overview

The simplified internal block diagram of the P9222-R/RN is shown in Figure 2. Energy is transferred wirelessly from the transmitter to the P9222-R/RN via an external Rx coil and C_S capacitor(s). The external LC is connected to the AC1 and AC2 pins to be full-wave-rectified (AC-to-DC).

5.1.1 Low-Power Ping Detection

Once charging has completed, the wireless power connection to the Tx can be programmed to terminate to save power. In order to inform the system that the P9222-R/RN is still on the charger, the PDETB pin will be held LOW as long as Tx ping pulses are detected. The resistor and capacitor (RC) connected to the PDET_RC pin should be selected such that the time constant of the RC maintains an adequate charge between Tx ping events to prevent PDETB from changing states until the device is removed from the Tx. The values of the RC circuit should be selected based on the expected ping time interval of the Tx. For more information, see “Low-Power Ping Detection Operation”.

5.1.2 Rx Operation

The wireless power is stored on a capacitor(s) connected to the VRECT pin in Rx mode. Until the voltage across the VRECT capacitor exceeds the under-voltage lock-out (UVLO) threshold, the rectification is performed by the body diodes of the synchronous full bridge rectifier FETs. After the internal biasing circuit is enabled, the driver and control blocks operate the MOSFET switches of the rectifier in various modes to maintain reliable connections and optimal efficiency. An internal ADC monitors the voltage at VRECT and the load current. The P9222-R/RN sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission based on these readings. The LDO VOUT pin can be pre-programmed from 3.5V up to 12V or changed after startup using I^2C commands. The headroom and target VRECT value will automatically adjust based on the latest VOUT set-point programmed value. The internal temperature is continuously monitored to ensure proper operation.

5.2 Wireless Power Control

The voltage at VRECT and the current through the rectifier are sampled periodically and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the internal control logic, which decides whether the loading conditions on VRECT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at VRECT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO’s load current increases.

5.3 Startup

When a mobile device containing the P9222-R/RN is placed on a WPC “Qi” charging pad, it responds to the transmitter’s “ping” signal by rectifying the AC power from the transmitter and storing it on a capacitor connected to VRECT. During the “ping” phase, once the rectifier provides a voltage at the VRECT pin above the UVLO threshold, the digital section of the P9222-R/RN enables communication. The control loop of the P9222-R/RN adjusts the rectifier voltage by sending Control Error Packets (CEPs) to the transmitter before and after it enables the VOUT LDO.

The VOUT LDO is enabled when the power transfer phase is initiated and the voltage at VRECT (i.e., the output of the full-wave synchronous rectifier reaches the target voltage that includes headroom in addition to the LDO VOUT target voltage). For example, if the VOUT voltage target is 5V, the target VRECT voltage is VOUT plus headroom. If the VRECT target voltage is not reached within 1 second after entering the power transfer phase, the VOUT LDO will be enabled automatically.

5.4 Power Transfer

Once the "identification and configuration" phase is completed then the transmitter initiates the power transfer mode. The P9222-R/RN control circuit measures the rectifier voltage, sends CEPs to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator, and sends Received Power Packets (RPPs) to notify the Tx of the current for foreign object detection (FOD) to guarantee safe, efficient power transfer. For more information about WPC-compliant power transfer, see "WPC-Compliant Power Transfer."

5.5 Synchronous Rectifier

The efficiency of the full-bridge rectifier in the P9222-R/RN is increased by operating in full synchronous rectifier mode. The rectifier is comprised of four self-driven switches that work in a full synchronous mode of operation when the load is higher than a programmable level (typically 150mA for BPP operation). Below that threshold, the rectifier works in half-synchronous rectification mode. At power-up, when the voltage is below the UVLO threshold, the rectifier functions by using the body diodes associated with the NMOS transistors. The BST capacitors are used to provide power to drive the gates of the high-side NMOS switches.

5.6 Over-Voltage Protection

In the event that the input voltage increases above 15V (default setting), the Rx sends control error packets to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level while simultaneously clamping the incoming energy using the internal high voltage OVP FET for VRECT over-voltage clamping control. The clamp is released when the VRECT voltage falls below the V_{OVP} hysteresis falling level. The P9222-R/RN also sends interrupts to the application processor (AP) when the over-voltage event occurs.

5.7 Over-Current Protection and Thermal Shutdown

The P9222-R/RN uses over-current and thermal protection by sending an interrupt to the AP to notify the host controller if the output current or die temperature has exceeded the operating limits. In the event that an overcurrent condition exists, the interrupt is sent to the AP with the expectation that it will respond by reducing the output consumption being drawn from the P9222-R/RN. If the overcurrent condition persists and is not corrected, then P9222-R/RN die temperature increases can be expected. In the event that the die temperature exceeds the thermal shutdown level, an End Power Transfer packet is sent to the transmitter to terminate power transfer and protect the P9222-R/RN from thermal stress. The current limit level is programmable. The P9222-R/RN sends interrupts to the AP if the current limit is reached or the die temperature reaches elevated levels to allow the AP an opportunity to reduce the load current in order to prevent power transfer interruptions.

5.8 External Temperature Sensing

The P9222-R/RN includes an optional temperature sense input pin on GP0. It is used to monitor a remote temperature, such as on an Rx coil or a PC board using an external thermistor circuit shown in Figure 15.

The GP0 pin voltage can be calculated using the following equation,

$$\boldsymbol{V_GP0 = V_LDO1P8 \times \frac{NTC}{R21+NTC}} \qquad \text{Equation 1}$$

where NTC is the thermistor's resistance (RTH1) and R21 is the pull-up resistor connected to the 1.8V (LDO1P8) supply voltage on the P9222-R/RN Evaluation Board. The over-temperature interrupt is triggered if the voltage on the GP0 pin is lower than 0.6V. The RTH1 is not populated on the P9222-R/RN Evaluation Board.

Figure 15. RTH1 and R21 Schematic Location

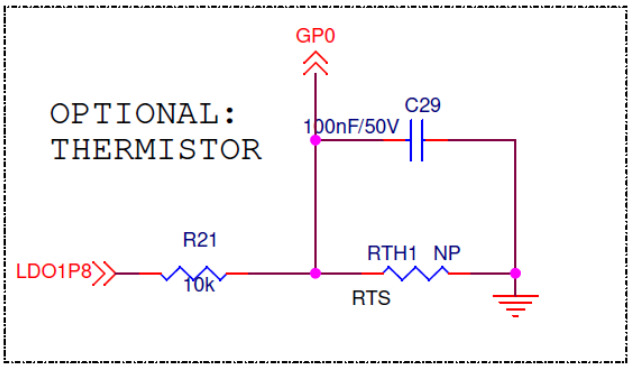
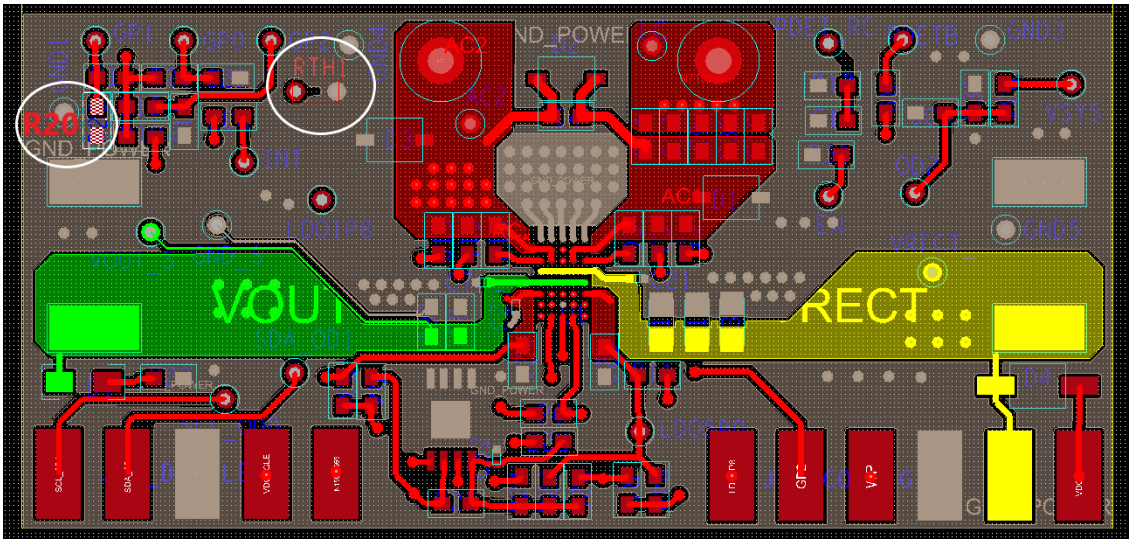


Figure 16. RTH1 and R21 PCB Location



5.9 Rectifier and VRECT Level

Once VRECT powers up to greater than UVLO, the full-bridge rectifier switches to half synchronous or full synchronous mode (depending on the loading conditions) to efficiently transfer energy from the transmitter to the load applied to VOUT. The VRECT pin must not be directly loaded. The rectified voltage will automatically self-adjust based on the programmed output setting to regulate throughout for all phases of charging to maintain adequate headroom that is balanced with optimal efficiency.

5.10 Interrupt Output

In Wireless Power RX mode, the /INT pin can be programmed to go LOW to indicate that an over-current, over-voltage, or over-temperature event has occurred. This feature is programmable and can be implemented using the /INT.

5.11 Low Drop-Out (LDO) Regulators

The P9222-R/RN has three LDO regulators. The primary VOUT LDO is powered by VRECT. The VOUT LDO can be programmed to any voltage between 3.5V and 10V; however, the output voltage setting should be compatible with the wireless Tx capability and coil type. The LDO5P0 is powered directly from VRECT, and LDO1P8 is powered from LDO5P0. Both are used for supplying power to internal low-voltage blocks. The LDOs must have local ceramic bypass capacitors placed near the P9222-R/RN. For recommended values, follow the application schematic in Figure 36.

5.12 MLDO Output Enable Conditions

After the P9222-R/RN is energized wirelessly by a valid Tx and reaches the power transfer state, there are two criteria that must be met prior to the VOUT MLDO regulator being automatically enabled after start-up. Upon connection to a Tx, the P9222-R/RN sends CEP +55 in order to drive VRECT up to 6.5V and also starts a 1-second timer to allow VRECT to reach the target. After this timer expires, one of two conditions must be met before the VOUT output is enabled: CEP values are less than +4 (indicates VRECT has reached the target), or 5 seconds pass. Either of these events will trigger the P9222-R/RN to enable VOUT. In cases where VRECT is still below the target voltage (5 seconds pass and VRECT < Vrect_Target), VOUT is enabled in order to allow charging to start. When VRECT is below Vrect_Target, full power charging may not be possible because the Tx is not providing adequate energy for full power to be transferred.

5.13 Output Power Options

The P9222-R/RN supports configurations such as described in the WPC Baseline Power Profile (BPP) specification. The P9222-R/RN can be programmed to optimize power delivery for low-power wearable applications and can also provide VOUT and VRECT battery voltage tracking to reduce losses, further improving efficiency and reducing heat generation during charging.

6. Bi-directional User Data Communication

Note: The default firmware supports bi-directional user data communication.

In customer-end systems, the transmitter and receiver boards must have an external microcontroller (MCU) or leverage an existing application processor to orchestrate bi-directional communication. Using the I2C communication, the MCU on the receiver board must load the data into specific registers and trigger the communication. The P9222-R/RN sends the data to the P9235-RB using amplitude-shift keying (ASK) modulation. The P9235-RB will receive the data and interrupt the MCU on the transmitter when the data is ready to be read. The external MCU on the transmitter follows the same procedure to send the data to the P9222-R/RN. When new data is available to be read, the P9222-R/RN will interrupt the external MCU on the receiver board.

Bi-directional user data communication is enabled only in the power transfer phase for the WPC standard. The external MCU on the receiver board can read register 0x4C (bit 0) to determine whether the P9222-R/RN is in the power transfer phase.

See Figure 19 for a state diagram that shows the procedure that the external MCU on the receiver board must follow to send the user data from the P9222-R/RN to the P9235-RB as described in "Transferring Data from the P9222-R/RN to the P9235-RB." See Figure 20 for a state diagram that shows the procedure that the external MCU must follow to read the data sent by the P9235-RB as described in "Reading Data Sent from the P9235-RB to the ".

6.1 Transferring Data from the P9222-R/RN to the P9235-RB

The external MCU on the receiver board should read bit 5 in register 0x4C to determine the status of the communication channel before initiating a new transfer. If the communication channel is free, bit 5 in register 0x4E is 0. If the communication channel is busy, bit 5 in register 0x4E is set to 1. The P9222-R/RN receiver supports sending up to 7 bytes of user data. The external MCU on the receiver should write the data that it will send to the transmitter into the Outgoing User Data Registers (0x51 to 0x57) and set the Data Header register (0x50) accordingly.

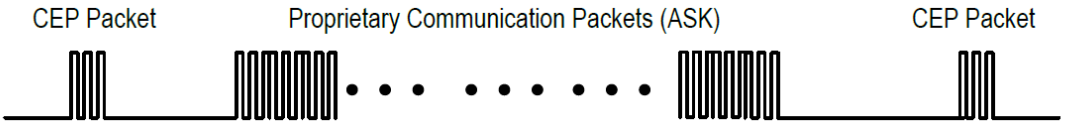
Table 6. Registers Used for Data Transmission from P9222-R/RN to P9235-RB

Register Name	Register Address
Command Register	0x4E
Data Header Register	0x50
Outgoing User Data Registers	0x51 to 0x57 (7 bytes)
System Mode register	0x4C
Power Transfer Phase Indicator	0x4C (bit 0)

The external MCU on the receiver should set bit 0 in the Command register 0x4E to 1b to trigger the communication after loading the user data into the outgoing data registers and setting the data header for the correct number of bytes. If the receiver is sending 1 byte, 2 bytes, and 3 bytes in the outgoing register, then the user would set the header register to 0x18, 0x28, and 0x38, respectively. After receiving the communication trigger from the control register, the P9222-R/RN reads the data header register and outgoing data registers and constructs a proprietary communication packet with a packet checksum. The communication packet is sent into the channel between two Control Error Packets (CEP) using ASK modulation.

Figure 17 shows the timing diagram for the user data transfer from the P9222-R/RN to the P9235-RB.

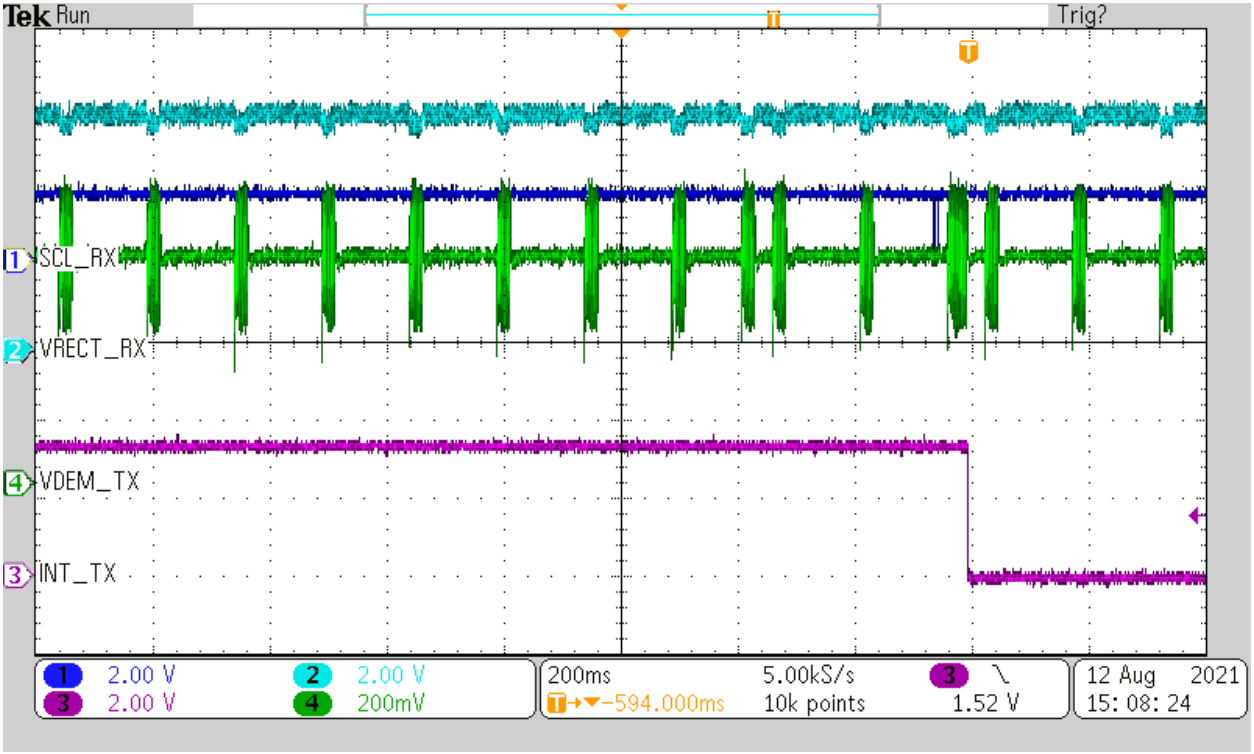
Figure 17. Timing Diagram for a User Data Transfer from the P9222-R/RN to the P9235-RB



The P9222-R/RN transfers data into the channel at a speed of 2Kbps. However, the channel is usually busy transmitting WPC standard communication packets. There is a very small window in which the user data can be transferred. Typically in the power transfer phase, the CEP packet is sent every 150msec. In one second, there will be only 6 to 7 time slots in which the P9222-R/RN can send a maximum of 7 bytes (including the checksum and header) of user data in each slot. The maximum data transfer rate achieved between the P9222-R/RN and the P9235-RB is 100bps. The P9222-R/RN will reset bit 0 in the Command register 0x4E to 0 immediately after sending the data into the channel. The external MCU on the receiver can periodically check bit 0 in the P9222-R/RN register 0x4E to get an acknowledgment of successful data transmission into the channel.

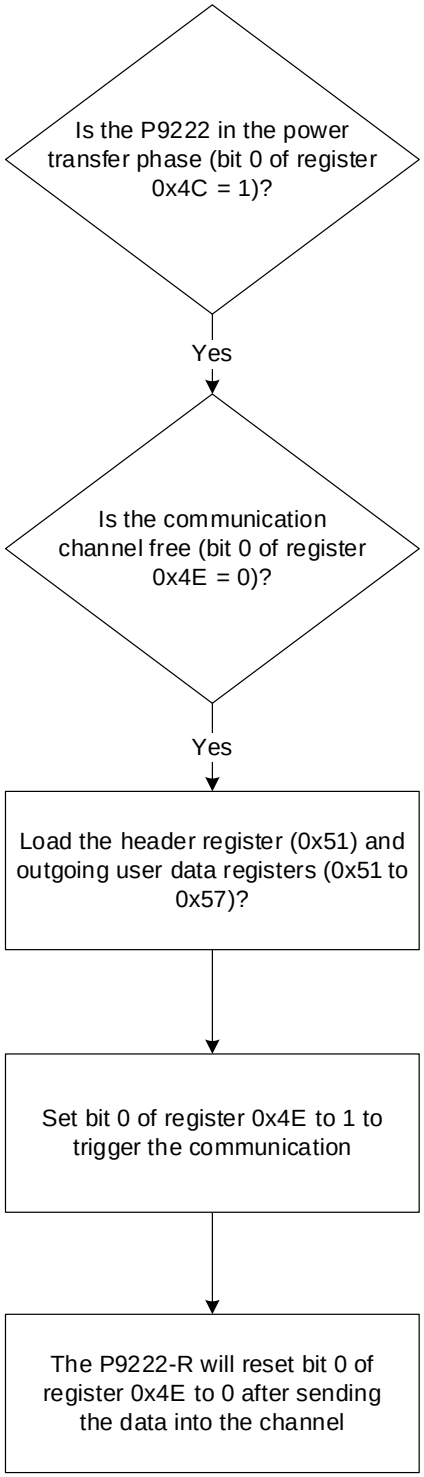
Note: The P9222-R/RN gives WPC standard communication packets priority over user data packets. User data packets have the lowest priority; therefore, during load transients, the P9222-R/RN may skip sending user data packets and give priority to CEP and indicate the channel status as busy in register 0x4E. The P9222-R/RN does not wait for acknowledgement from the P9235-RB or keep track of successful delivery of the data to the P9235-RB. The P9222-R/RN only functions as a messenger and relies on the external MCUs on the receiver and transmitter boards to create a lossless communication protocol by adding intelligence into data they are transferring.

Figure 18. Typical P9222-R/RN to P9235-RB Data Transfer using the P9235A-RB-EVK Evaluation Kit



Note: The P9235A-RB-EVK is the evaluation kit available for the P9222-R/RN and P9235-RB, which implements the typical application schematic shown in Figure 32.

Figure 19. State Diagram for User Data Transmission from the P9222-R/RN to the P9235-RB



If the receiver is sending 1 byte, 2 bytes, and 3 bytes in the outgoing register, then we would set the header register to 0x18, 0x28, and 0x38 respectively.

6.2 Reading Data Sent from the P9235-RB to the P9222-R/RN

The P9222-R/RN can receive 7 bytes of information at a time. When the P9222-R/RN receives the data from the P9235-RB, it will generate an interrupt to the external MCU on the receiver by pulling down the interrupt pin, INT. Because interrupts can be generated for multiple reasons, the MCU can respond to the data received interrupt and read the data received flag in bit 5 of System Interrupt register 0x36 and bit 5 of System Status register 0x34, respectively, to confirm that the interrupt is generated because of new incoming data. After confirming that new data is available to read, the external MCU can read incoming header register (0x57) and user data registers (0x58 to 0x5F).

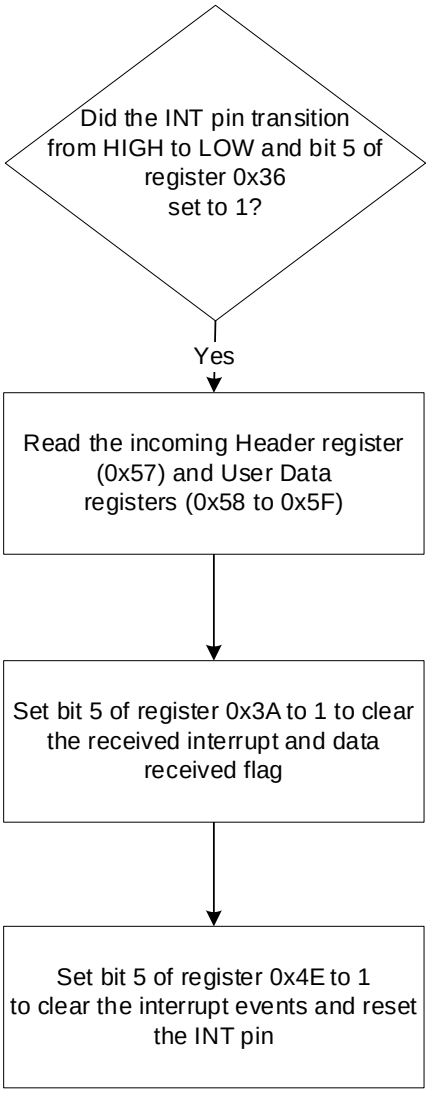
Table 7. Registers Used for Reading User Data from the P9235-RB

Register Name	Register Address
Command Register	0x4E
System Status Register	0x34
System Interrupt Register	0x36
Interrupt Enable Register	0x38
Interrupt Clear Register	0x3A
Clear Interrupt Events	0x4E (bit 5 set to 1)
Header Register	0x57
User Incoming Data Registers	0x58 to 0x5F (7 bytes)

Note: TX Data Received Interrupt Enable Register 0x38 bit 5 is disabled by default.

After reading the data, the external MCU on the receiver should clear the interrupt by writing 1 to bit 5 in Interrupt Clear Register 0x3A, which clears the data received interrupt and data received flag. Afterwards, bit 5 in the Command Register (0x4E) should be set to 1b to instruct the processor to clear the interrupt events. If the interrupt event is not cleared, the P9222-R/RN will reject new incoming data because old data was not read by the MCU on the receiver. The user can implement a higher-level handshaking protocol between the external MCU on the transmitter and the receiver to avoid data corruption.

Figure 20. State Diagram for Reading User Data Received from the P9235-RB



If the receiver is sending 1 byte, 2 bytes, and 3 bytes in the outgoing register, then we would set the header register to 0x18, 0x28, and 0x38 respectively.

7. WPC Mode Characteristics

For a description of the startup process for wireless charging, which is compliant with the WPC protocol, see “Startup”.

7.1 WPC-Compliant Power Transfer

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer phase. The P9222-R/RN control circuit measures the rectifier voltage and sends CEPs to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to notify the Tx of the current Received Power Packet for foreign object detection (FOD) in order to guarantee safe, efficient power transfer. The P9222-R/RN is compatible with WPC specification and can use compatible Rx coils. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitor (C_S) is used for a given type of receiver coil.

7.2 Advanced Foreign-Object Detection (FOD) in WPC Mode

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of parasitic metal objects are coins, keys, paperclips, etc. The amount of heating depends on the amplitude and frequency of the magnetic field coupled, as well as the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduced power transfer efficiency. Moreover, if no appropriate measures are taken, the heating could lead to unsafe situations if the objects reach high temperatures.

WPC power transmitters and receivers need to also compensate for the power loss due to parasitic metals intentionally designed into the final product; i.e., metals that are neither part of the power transmitter nor of the power receiver, but which absorb power from magnetic field coupling during the power transfer, such as Li-ion batteries, metallic cases, etc.

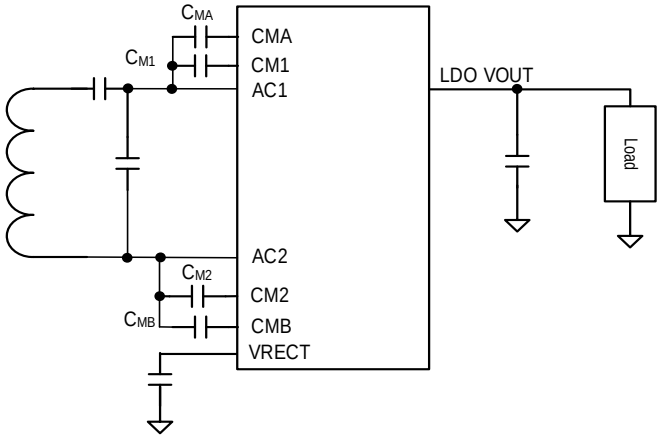
The P9222-R/RN uses advanced FOD techniques to detect foreign objects placed on or near the transmitter base station. The FOD algorithm includes values that are programmable through either the I2C interface or external EEPROM memory bits. Programmability is necessary so that the FOD settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the Tx and Rx coils, battery, shielding, and case materials under no load to full load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different from the expected system power.

The P9222-R/RN FOD values need to be tuned prior to production for WPC compliance using final production hardware and coils.

7.3 WPC Modulation/Communication

The P9222-R/RN operates in the WPC mode using a single LC tank Rx coil and requires AC modulation capacitor connections for WPC communication. The capacitors C_{M1} and C_{M2} (connected to pins CM1 and CM2 respectively; see Figure 21) and the LC tank accomplish WPC modulation. The capacitor values should be tuned to achieve maximum efficiency while still providing adequate communications.

Figure 21. Rx Modulation Components



Receiver-to-transmitter communication is accomplished by modulating the load applied to the receiver; i.e., amplitude-shift keying (ASK). To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is done with AC modulation, using internal switches to connect external capacitors from AC1 and AC2 to ground.

The P9222-R/RN communicates with the base station by sending ASK communication packets to WPC transmitters. Each communication packet has the following structure:

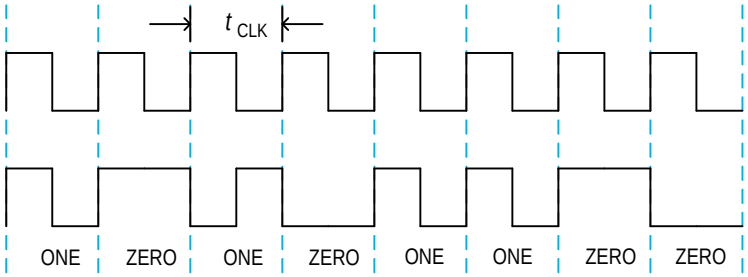
Figure 22. Communication Packet Structure

Preamble	Header	Message	Checksum

7.4 Bit Encoding Scheme for ASK

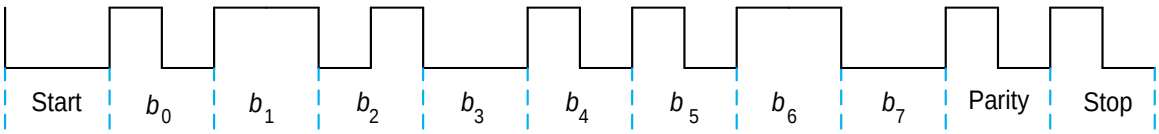
As required by the WPC specification, the P9222-R/RN uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using two wider transitions as shown in Figure 23.

Figure 23. WPC Packet Example with Reference Clock Shown



Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 24. Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

Figure 24. Byte Encoding Scheme



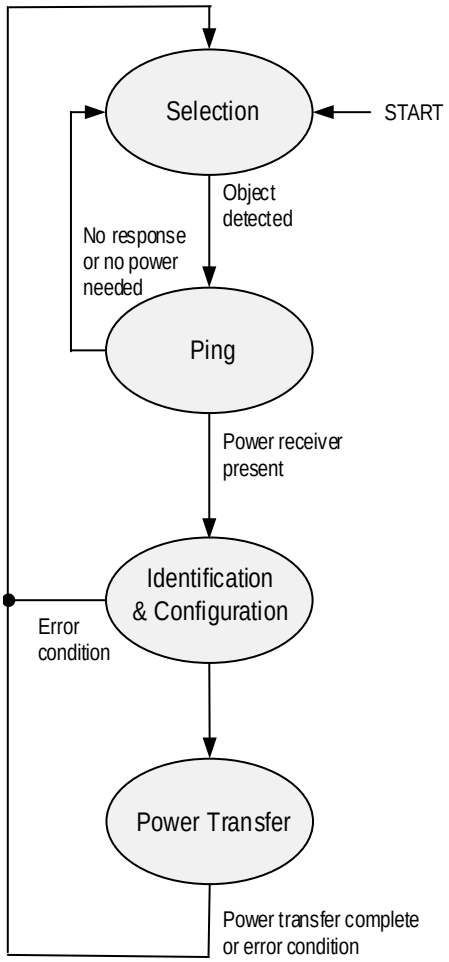
7.5 System Feedback Control

The P9222-R/RN is fully compatible with WPC (Baseline Power Profile) and has all the necessary circuitry to communicate with the base station via WPC communication packets. The overall WPC system behavior between the transmitter and the receiver follows the state machine shown in Figure 25.

The P9222-R/RN goes through four phases:

1. Selection
2. Ping
3. Identification and Configuration
4. Power Transfer

Figure 25. WPC System Feedback Control BPP Mode



7.5.1 Selection

In the “Selection” phase, the P9222-R/RN is prepared to sense or deliver the wireless power and proceeds to the “Ping” state. It monitors the rectified voltage, and when the voltage is above the V_{UVLO_RISING} threshold (see Table 5), the P9222-R/RN prepares to communicate with the base station or enter the power “Ping” phase.

7.5.2 Ping

In the “Ping” phase, the P9222-R/RN transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal on. After sending the Signal Strength Packet, the P9222-R/RN proceeds to the “Identification and Configuration” phase. If, instead, an End Power Transfer packet is sent or requested to be sent by the AP, or if an invalid response is sent, then the P9222-R/RN remains in the “Ping” phase.

In this phase, the P9222-R/RN sends the following packets:

- Signal Strength Packet
- End Power Transfer Packet

7.5.3 Identification and Configuration

In the “Identification and Configuration” phase, the P9222-R/RN sends or expects the following packets:

- Identification Packet
- Configuration Packet

After the transmission of the Configuration Packet, the P9222-R/RN proceeds to the “Power Transfer” phase.

7.5.4 Power Transfer

In the “Power Transfer” phase, the P9222-R/RN controls the power transfer by means of the following control data packets:

- Control Error Packets (CEP)
- Rectified Power Packet (RPP)
- End Power Transfer Packet (EPT)

7.5.4.1 End Power Transfer (EPT) Packet

In the event of an EPT, the P9222-R/RN turns off only after the AP instructs the P9222-R/RN to continuously send End Power Transfer packets until the transmitter removes the power and the rectifier voltage on the receiver side drops below the under-voltage lock-out (UVLO) threshold (see Table 5).

8. Applications Information

The P9222-R/RN is an integrated wireless power receiver for mobile or stationary devices. The device can receive and provide to its output up to 5W of wireless power using near-field magnetic induction.

8.1 Receiver Coil

The following coils are recommended for use in 5W or 3W applications in order to achieve optimum performance with the P9222 receiver.

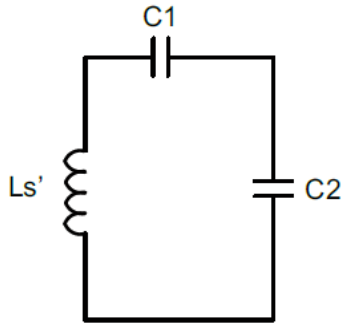
Table 8. Recommended Coil Manufacturer

Output Power	Vendor	Part Number	Inductance at 100kHz	Resonant Caps (Cs)	DC Resistance at 20℃
5W	SUNLORD	MQQRR303008S8R2	8.2µH ± 10%	300nF	180mΩ max
3W	TDK	WR303050-12F5-ID	8.2µH ± 10%	300nF	280mΩ max

8.2 Series and Parallel Resonant Capacitor Selection

WPC inductive power transmission uses resonant circuits to enhance the inductive power transmission. Especially for systems with a low coupling factor, a resonant receiver can improve power transfer. The simplified Rx-coil network consists of a series resonant capacitor, C1, and a parallel resonant capacitor, C2. These two capacitors make up the dual resonant circuit with the Rx coil (see Figure 26) and must be sized correctly as per the WPC specification.

Figure 26. Dual Resonant Circuits with Receiver Coil



To calculate C1, a 100kHz resonant frequency is used along with the measured L's values (Receiver Coil inductance measured when placed on the TX coil and shield)

$$C1 = \frac{1}{(100kHz \times 2\pi)^2 \times L'_s} \qquad \text{Equation 2}$$

To calculate C2, a secondary resonance of 1.0MHz is used along with Ls (Free space Receiver Coil inductance without TX coil and shield). This calculation requires that C1 be determined first and used in Equation 3:

$$C2 = \frac{1}{(1.0MHz \times 2\pi)^2 \times (Ls - \frac{1}{C1})} \qquad \text{Equation 3}$$

8.3 VRECT Pin

The efficiency of the full-bridge rectifier in the P9222-R/RN is increased by implementing it as a synchronous rectifier.

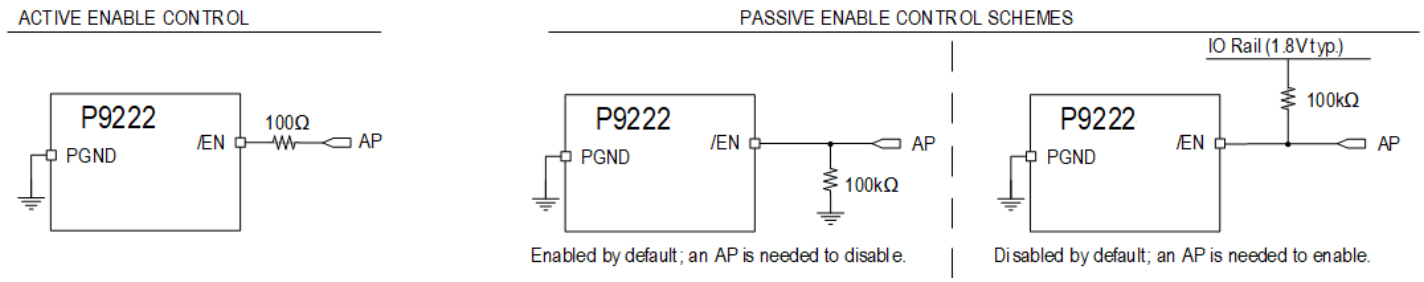
The rectifier comprises four self-driven switches that work in a full synchronous mode of operation when the load is higher than 150mA. Below that threshold, the rectifier works in half-synchronous rectification mode. At power-up, when the voltage is below the UVLO threshold, the rectifier works by using the body diodes associated with the NMOS transistors. The BST capacitors are used to provide power to drive the gates of high-side NMOS switches.

8.4 Enable Pin

The P9222-R/RN offers an active LOW enable function that allows the host AP to control when wireless power will be enabled. The /EN enable pin (C4) must be actively pulled-up or pulled-down using the AP to drive the pin directly, or by using an external resistor to passively control the default state. The /EN pin is a push-pull general purpose input/output (GPIO) type input and will consume current when driven HIGH while the P9222-R/RN is not powered. It is recommended that one of the circuits shown in Figure 27 be followed.

The /EN pin can be actively controlled (AP I/O directly connected to /EN pin) or passively controlled depending on system requirements. Since the AP must be used to control the P9222-R/RN enable pin, power will be consumed by the biasing resistor when the state is changed from the default if using a passive control scheme – this may be needed to support AP sleep modes. Typical systems will use the P9222-R/RN set up to be enabled by default in order to save the most power, and will disable wireless charging when wired charging is used or some other function is being performed that requires wireless charging to remain disabled. One of the diagrams in Figure 27 must be used to set the default /EN pin state for the P9222-R/RN.

Figure 27. P9222-R/RN Recommended Enable Default State Configurations



When using the “active enable control,” it is important to always force the /EN pin into a known state, and the /EN pin should never be left floating. For example, in some applications when the battery is dead or when the AP is in sleep mode, the AP may not be actively driving the /EN pin. In order to prevent the /EN pin from floating in such cases, a pull-down resistor should be added.

8.5 Transient Voltage Suppressor Diodes (TVS)

Transient Voltage Suppressor diodes can be added to the design from the AC1 and AC2 nodes to GND, or from AC1 to AC2 (D10, D2, D3, as shown in the reference schematic). This component is useful to rapidly limit incoming ESD surges, or situations when the Tx incoming power exceeds the expected power and Vrect voltage rises above target and over 15V in less than 10µs to aid in voltage limiting the incoming AC waveforms. A balance in Reverse Standoff Voltage (V_{RWM}), Clamping Voltage (V_{CL}), Break-down Voltage (V_{BR}) relative to the expected Vrect operating voltage Vrect (be sure minimum V_{BR} is less than maximum operating Vrect value and that V_{CL} is less than Vrect Absolute maximum voltage) should be reached. The following guidance should be used for the P9222-R/RN when selecting TVS diodes:

- V_{RWM} = 12V maximum
- V_{BR} = 14.6 V minimum at 5mA
- V_{CL} = 22 V maximum at 1App

When TVS diodes are used, it is recommended to place them as close to the coil on the respective nodes as possible to shunt high voltages away from the P9222-R/RN. Zener diodes can also be used to limit voltage levels, and the Zener voltage should be above the working voltage of the node and below the absolute maximum voltage of the pin connected to the node.

8.6 GPIO Pins

The P9222-R/RN has general-purpose input output (GPIO) pins for custom applications. The OD0-OD2 and GP0-GP2 pins are all multi-functional. In addition, OD0-OD2 have an open-drained structure and GP0-GP2 have a push-pull structure.

8.6.1 OD0 Pin

The OD0 pin has a digital function open-drain structure. It is assigned to SCL of I2C function for the serial interface between the AP and the P9222-R/RN. An external pull-up register on the SCL line is required for I2C communication. OD0 can operate up to 5V.

8.6.2 OD1 Pin

The OD1 pin has a digital function open-drain structure. It is assigned to SDA of I2C function for the serial interface between the AP and the P9222-R/RN. An external pull-up register on the SDA line is required for I2C communication. OD1 can operate up to 5V.

8.6.3 OD2 Pin

The OD2 pin is connected to the internal ADC and can measure voltage levels smaller than 1.2V. The register address is 0xD4 with 16-bit long data. The value is always in ADC counts and therefore must be converted to the desired units. For the conversion is:

AdcResult[0] * 2100 / 4096 = Voltage on OD2 in mV

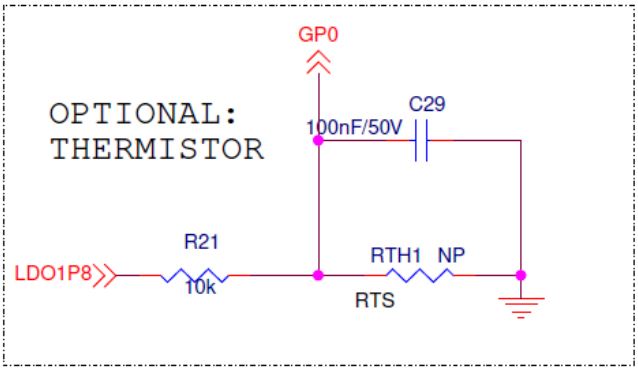
The OD2 absolute maximum voltage rating is 2V. Care should be taken that the OD2 pin level is always below 2V. If the ADC function is not used, this pin can be left floating.

8.6.4 GP0 Pin

The GP0 pin is connected to the internal ADC and can measure external temperature on either the receiver coil or the PCB with an external thermistor circuit.

The P9222-R/RN sends interrupts to the AP if the temperature reaches the threshold level (0.6V default, configurable) to allow the AP an opportunity to reduce the temperature in order to prevent power transfer interruptions.

Figure 28. GP0 Pin External Connection to Thermistor Configuration



If external temperature sensing is not used, pull this pin to 1.8V (LDO1P8) with a resistor.

8.6.5 GP1 Pin

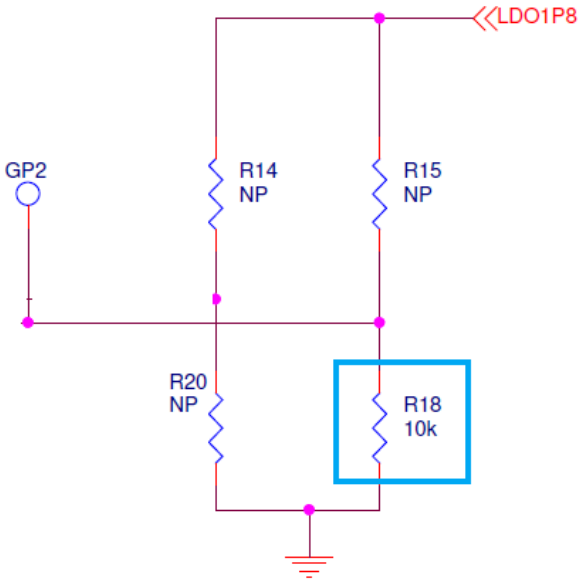
The GP1 pin is connected to the internal ADC and can measure the voltage smaller than 1.8V. The register address is 0xD6 with 16-bit long data. The value is always in ADC counts and therefore must be converted to the desired units. For the conversion is:

AdcResult[1] * 2100 / 4096 = Voltage on GP1 in mV

8.6.6 GP2 Pin

The GP2 pin is assigned as a digital input. If GP2 is asserted high, the P9222-R/RN will access an external EEPROM on the I2C bus and load customer configuration (FOD parameters, Vout, Ilim, and etc) data. If GP2 is asserted Low (default mode), the P9222-R/RN will load default configuration data from an internal NVM (OTP).

Figure 29. GP2 Pin External Connections for External EEPROM Selection



8.7 Low-Power Ping Detection Operation

Once charging has completed, the wireless power connection to the Tx can be ended using an End Power Transfer (EPT) packet to save power and reduce over heating of the device. The P9222-R/RN can be used to notify the host application processor that it is still on the charging pad by using the PDETB and PDET_RC pins. The PDETB pin should be externally pulled up and will be held LOW as long as Tx ping pulses are detected. The RC connected to the PDET_RC pin should be selected based on the expected ping time interval of the Tx. To prevent the P9222-R/RN from waking the AP prematurely during Ping Detect mode, the RC values should be selected to hold the PDETB pin LOW until a few hundred milliseconds after the expected ping interval from the Tx.

Figure 30. Ping Detection – Typical Application Schematic Components and Connections

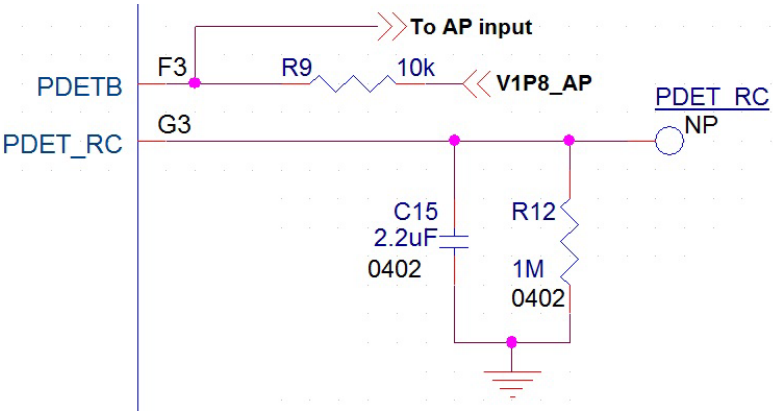
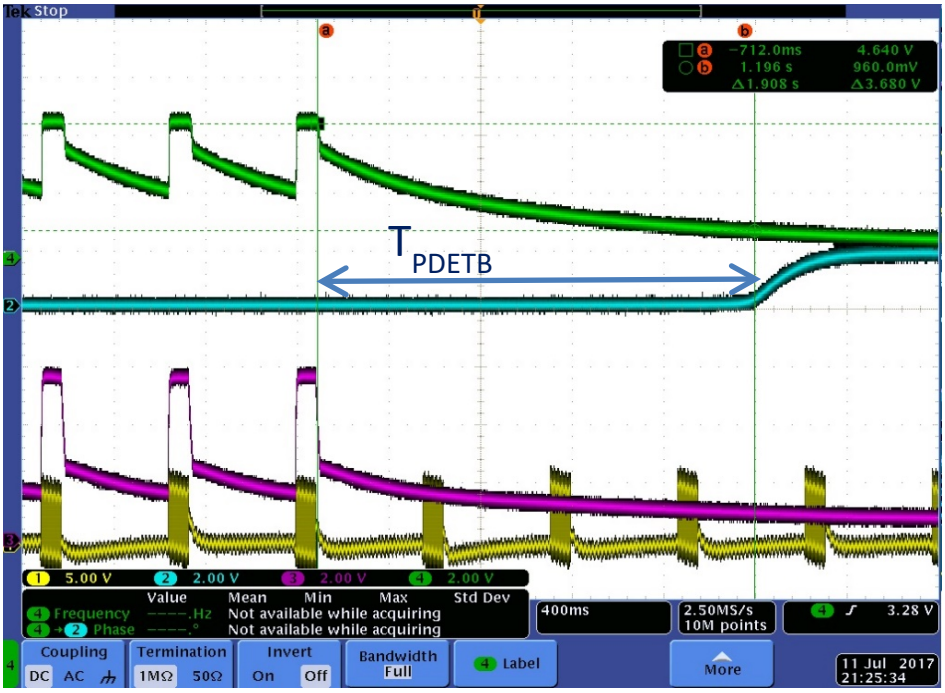


Figure 31. P9222-R/RN Ping Detect Waveforms[1]



Note: When measuring the PDET_RC node, the probe impedance will alter the timing of PDETB, and this should be accounted for.

Table 9 can be used to select the RC values for the PDET_RC pin.

Table 9. Recommended RC Values for PDET_RC Components Based on Capacitance and Ping Interval

Ping Interval (s)	R (MΩ)	C (µF)	T_{PDETB_MIN} (s)	T_{PDETB_MAX} (s)
0.55	0.422	2.2	0.66	1.36
0.75	0.59	2.2	0.92	1.89
0.9	0.698	2.2	1.098	2.26
1.2	0.887	2.2	1.38	2.85
	0.412	4.7	1.37	2.83
1.4	1.1	2.2	1.71	3.54
	0.511	4.7	1.70	3.51
2.2	1.69	2.2	2.64	5.45
	0.787	4.7	2.62	5.41
6.5	5.11	2.2	7.95	16.43
	2.32	4.7	7.80	16.12

[1] R12 = 1MΩ, C15 = 2.2µF, Ch1 = Tx SW Node, Ch2 = PDETB, Ch3 = VRECT, Ch4 = PDET_RC, 25°C, 550ms Ping Interval

8.8 Configuration of P9222-R/RN Parameters

The P9222-R/RN firmware provides great flexibility to customize operating parameters for custom applications. Default values of the P9222-R/RN operating parameters such as output voltage, FOD parameters, and current limit are set in the firmware programmed into the internal one-time programmable (OTP) memory. Based on the end application, the P9222-R/RN operating parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by loading the user configuration generated by the P9222-R/RN GUI into an external EEPROM.

The register map in “Registers” describes all the SRAM registers that can be configured via the I2C interface. The SRAM registers content is volatile and all the content resets to default after every power cycle. The AP must update the operating parameters after every power cycle. The AP can use the VRECTON interrupt or battery charger interrupt as a trigger to update the SRAM registers.

If the end application does not have an external AP to update operating parameters, a generic purpose external EEPROM with I2C interface can be connected to the P9222-R/RN I2C port, and the GP2 pin needs to be tied to LDO1P8 using a 10K resistor. Using the P9222-R/RN Windows GUI, the operating parameters can be customized and a custom configuration file for the external EEPROM can be generated. The configuration file can be loaded into the external EEPROM using the I2C interface and the P9222-R/RN Windows GUI. Write protect on EEPROM needs to be disabled before writing the configuration to the external EEPROM.

If the GP2 pin is tied to LDO1P8, the P9222-R/RN accesses the external EEPROM during startup before turning on the main output LDO, and then sets the default operating parameters to the values set in the external EEPROM configuration.

8.9 P9222-R/RN Internal Register Access by Application Processor

The user registers are located in the SRAM space starting from address 0x0000, and are accessible via the standard I2C interface. The P9222-R/RN I2C device address is 0x61.

Some of the registers are 2 bytes long (16-bit). The P9222-R/RN microprocessor updates the memory location by writing both bytes in a single clock. The I2C bus reads the bytes sequentially, and it is possible to split the read value between old and new value. If a critical decision must made based on a value, the register of interest needs to be read two or more times until the same number appears in two consecutive read operations. The Internal register map is listed in “Registers”.

8.10 External EEPROM Access by P9222-R/RN

An external EEPROM with an I2C interface can be connected to the P9222-R/RN I2C pins, and the user configuration generated from the P9222-R/RN Windows GUI can be loaded into the external EEPROM to configure the default values of the P9222-R/RN operating parameters (e.g., FOD parameters). The P9222-R/RN polls the GP2 state during startup. If the GP2 pin is high, the P9222-R/RN will become an I2C master and quickly read 100 bytes of the user configuration data from the external EEPROM. After reading the data, the P9222-R/RN will revert back to its default I2C slave state and then check the data integrity of the read data using a checksum calculation. If the data checksum matches correctly, the P9222-R/RN overrides the default values of the operating parameters set in the OTP firmware with the new values from the external EEPROM. If the data checksum does not match, the P9222-R/RN continues to use the default values of the operating parameters set in the OTP firmware. Register 0xD2 can be polled to check whether the P9222-R/RN is using the configuration from an external EEPROM or the default OTP configuration.

The external EEPROM I2C device address is 0x50. The 24AA128T external EEPROM is used in the P9222-R/RN reference design. A0, A1, and A2 pins are tied to GND in the design. Write-protect must be disabled while the user configuration in the external EEPROM is updated.

An external EEPROM to configure the operating parameters is typically used when there is no I2C master in the application accessing the P9222-R/RN. If there is another I2C master on the same I2C bus that the P9222-R/RN and external EEPROM is also using, it is recommended to add an I2C switch to avoid potential I2C bus contention.

9. Examples of User Customizing P9222-R/RN Operating Parameters

9.1 LDO Output Voltage (VOUT) Configuration

The default VOUT voltage of the P9222-R/RN is 5.0V. The user can change the default Vout voltage in accordance with specific user design requirements and store the modified configuration in the external EEPROM, or an external AP can adjust VOUT voltage continuously via the I2C interface. In addition, an external MCU can continuously read the battery voltage and change VOUT to lower the losses in the battery charger to optimize the total system efficiency. The P9222-R/RN configurable Vout voltage range is from 3.5V to 12V.

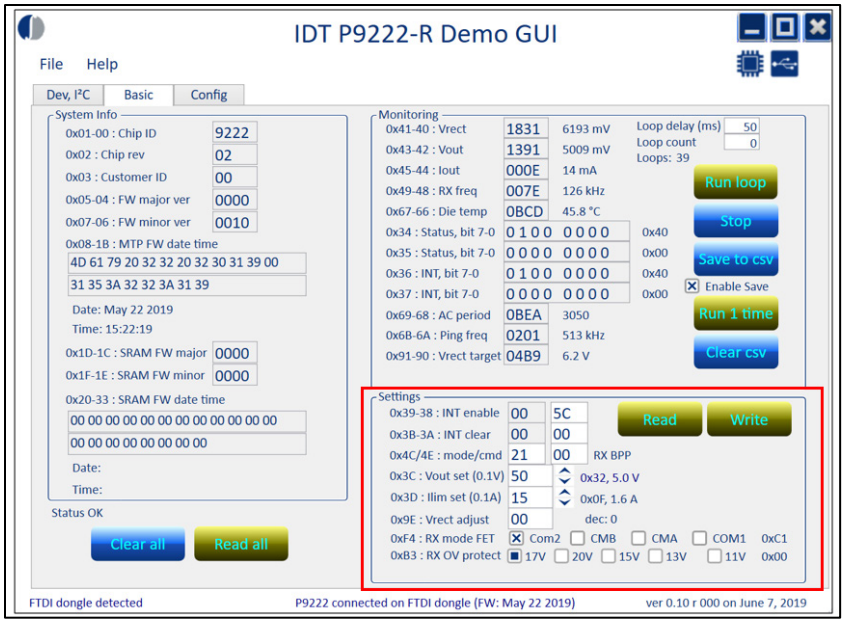
9.1.1 VOUT Adjustment via the I2C Interface

The P9222-R/RN output voltage can be changed by writing to the Vout_Set register (0x3C). The P9222-R/RN firmware reads the internal register value in regular time base and updates the Vout voltage. The output voltage can be incremented in steps of 100mV.

$$\boldsymbol{Output\ Voltage\ (VOUT) = \text{Deciamal Value of 0x3C register} * 0.1\ (\mathbf{V})} \qquad \text{Equation 4}$$

To change the 0x3C register using the P9222-R/RN Windows GUI, go to the VOUT voltage box in the GUI “Basic” tab (see Figure 32).

Figure 32. Writing to the Vout_Set Register using P9222-R/RN Windows GUI

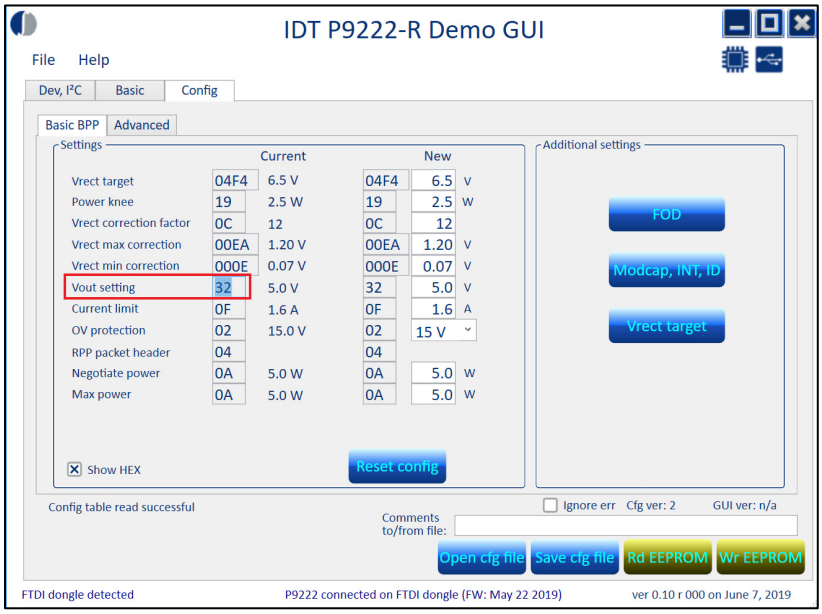


9.1.2 VOUT Configuration Change Using an External EEPROM

The default output voltage can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R/RN Windows GUI. To generate a new configuration file using the P9222-R/RN Windows GUI:

1. Place receiver with the P9222-R/RN on the WPC transmitter or apply 5V from an external power supply on VRECT node.
2. Launch the P9222-R/RN GUI, go to the “Config” tab, and then click on the “Rd EEPROM” button. The current EEPROM configuration values will be displayed.
3. Enter a new VOUT value and generate a new configuration by clicking on “Save cfg file”.
4. The Configuration can also be directly written to the external EEPROM by clicking “Wr EEPROM”. Write Protect on the EEPROM needs to be disabled before writing to the EEPROM.
5. After saving the new configuration into the EEPROM, the P9222-R/RN must be power cycled for the output voltage to change to the new value.

Figure 33. Changing the Default VOUT Value using the P9222-R/RN Windows GUI



9.2 Current Limit (ILIM) Configuration

The current limit threshold value is used to limit the output current of main LDO on the VOUT pin. If the output current reaches the target limit value, the P9222-R/RN will reduce the output voltage without increasing current. The default ILIM value of the P9222-R/RN is 1.6A. The user can change the default current limit value in accordance with specific user design requirements and store the modified configuration into an external EEPROM. In addition, after the P9222-R/RN enters the power transfer phase, an external AP can adjust the ILIM value by writing to the ILIM_Set register (0x3D) via the I2C interface. The P9222-R/RN firmware reads the internal register value in regular time base and updates the current limit value. The current limit can be incremented in steps of 100mA.

$$Current\ Limit\ (ILIM) = \text{Decimal Value of 0x3D register} * 0.1\ (\text{A}) \qquad \text{Equation 5}$$

The default Current Limit value can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R/RN Windows GUI. For information on how the configuration file can be generated using the P9222-R/RN Windows GUI, see “VOUT Configuration Change Using an External EEPROM.”

9.3 Overvoltage (OV) Protection Configuration

The wireless charging receivers are vulnerable to external high voltage condition (> 20V) caused by coupling factor changes or other abnormal behavior of rogue wireless power transmitters. The overvoltage protection function should be carefully configured to protect the receiver from worst cases. The overvoltage protection limit sets the maximum allowable Vrect voltage. If Vrect reaches the voltage limit (default OV voltage is 15V), the P9222-R/RN will do the following:

1. Turn on the internal clamping circuit
2. Enable an additional DC load when Vrect reaches 90% of the set level
3. Send an End Power Transfer packet (OV) to TX

The default OV protection limit value can be configured by writing a configuration file into the external EEPROM. The configuration file can be generated using the P9222-R/RN Windows GUI. For information on how the configuration file can be generated using the P9222-R/RN Windows GUI, see "VOUT Configuration Change Using an External EEPROM."

In addition, an external AP can adjust overvoltage protection limit by writing to the OV Set register (0x4C) via the I2C interface.

9.4 FOD (Foreign Object Detection)

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an unsafe temperature.

During the power transfer phase (see Power Transfer), the receiver periodically communicates to the transmitter the amount of power received by means of a Received Power Packet (RPP). The transmitter will compare this power with the amount of power transmitted during the same time period. If there is a significant unexplained loss of power, then the transmitter will shut off power delivery because a possible foreign object might be absorbing too much energy.

For a WPC system to perform this function with sufficient accuracy, both the transmitter and receiver must account and compensate for all of their known losses. Such losses, for example, could be due to resistive losses or nearby metals that are part of the transmitter or receiver. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (PPR) in an RPP. The maximum value of the received power accuracy $P\Delta$ depends on the maximum power of the power receiver as defined in Table 10.

The power receiver must determine its PPR with an accuracy of $\pm P\Delta$, and report its received power as PRECEIVED = PPR + $P\Delta$. This means that the reported received power is always greater than or equal to the transmitted power (PPT) if there is no foreign object (FO) present on the interface surface.

Table 10. Recommended Maximum Estimated Power Loss

Maximum Power (W)	Maximum $\boldsymbol{P\Delta}$ (mW)
5	350

The compensation algorithm includes values that are programmable via either the I2C interface or OTP bits. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

9.4.1 Configuring FOD Parameters

FOD parameters consist of 8 sections. Each section is divided by output current and consists of gain and offset to compensate for Rx internal power loss; each section is also adjusted for Reported Rx power. The following comprises the mA ranges for the FOD sections:

- FOD section [0] is from 0mA to 191mA
- FOD section [1] is from 192mA to 351mA
- FOD section [2] is from 352mA to 511mA
- FOD section [3] is from 512mA to 671mA
- FOD section [4] is from 672mA to 819mA
- FOD section [5] is more than 820mA

The formula of Rx Reported Power is:

$$Rx\ Reported\ Power[0..5] = Power(Rx\ delivered\ power) * FOD\ Gain[0 \ldots 5] + Offset[0..5] \qquad \text{Equation 6}$$

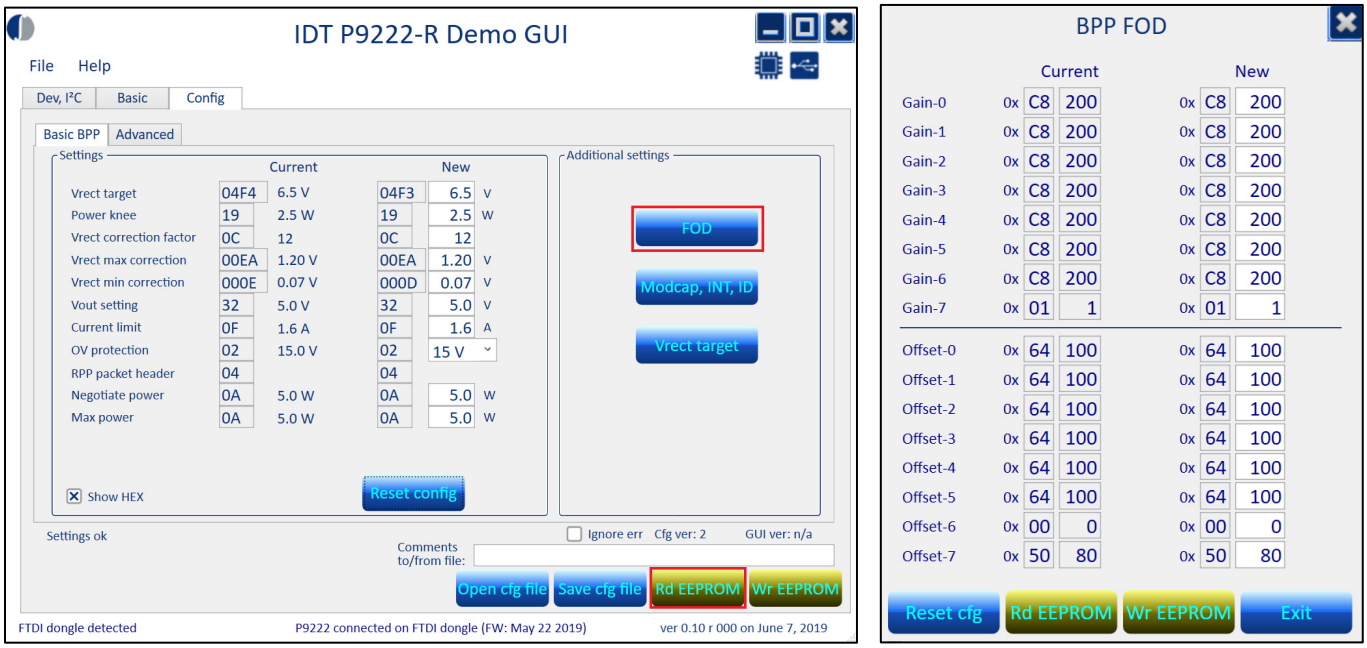
Place the receiver with the P9222-R/RN on the Nok9 FOD transmitter. Ramp the current on the output of the P9222-R/RN in steps of 50mA to 100mA and monitor power difference between the Nok9 transmitted power and the receiver reported power value. The difference should be within 0-350mW. If the difference exceeds 350mW, adjust the FOD gain or FOD offset of that particular output current section in order to bring the difference back to 0-350mW range. The AP can modify the FOD gain and FOD offset by writing to the Foreign Object Detection Registers (0x70-0x7E). In the final product, the AP can use the VRECTON interrupt or battery charger interrupt as a trigger to update the FOD registers.

The default values of the FOD registers can also be configured by the following writing a configuration file into the external EEPROM. To generate the configuration file using the P9222-R/RN Windows GUI:

1. Place the receiver with the P9222-R/RN onto the WPC transmitter or apply 5V from an external power supply on the VRECT node.
2. Launch the P9222-R/RN GUI, go to the “Config” tab, click the “Rd EEPROM” button, and then click the “FOD” button. A new popup window with the current FOD values stored in the external EEPROM will be displayed.
3. Enter new FOD values and click on the “Save cfg file” to generate a new configuration.

   The configuration can also be directly written into the external EEPROM by clicking the “Wr EEPROM” button. Note: The Write Protect function on the EEPROM must be disabled before writing to the EEPROM.

Figure 34. Changing the Default FOD Registers using the P9222-R/RN Windows GUI



9.4.2 Modulation Capacitor and Interrupt Enables

The P9222-R/RN sends the communication packets to the transmitter using ASK modulation of the coil voltage. For ASK modulation, the P9222-R/RN switches on and off the capacitors on the COM1, COM2, CMA, and CMB pins using internal MOSFETs. By default, the P9222-R/RN switches only MOSFETs on the COM1 and COM2 pins. ASK modulation depth can be increased by enabling the switches on the CMA and CMB pins. Measure the modulation depth on the transmitter demodulation circuitry, and if too small, adjust the ASK modulation depth by enabling the CMA and CMB switches. Modulation depth can also be increased by increasing the capacitor value. The AP can also change the ASK modulation depth by writing to the ASK modulation depth Registers (0xF4).

Using the /INT pin, the P9222-R/RN can interrupt the AP when there is a fault condition such as overcurrent or when there is a major state change such as when the VRECT is turned on. The AP can enable or disable the interrupt conditions by writing to the Interrupt Enable Registers, INT_Enable_L (0x38) and INT_Enable_H (0x39).

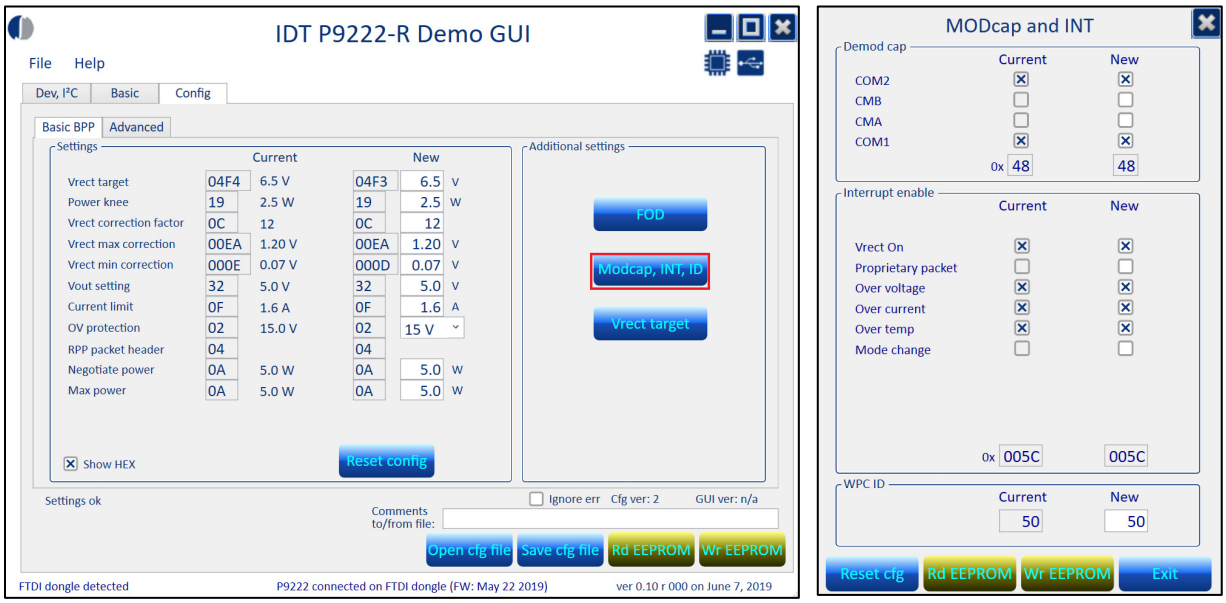
The default values of the ASK modulation depth and the interrupt enable registers can also be configured by writing a configuration file into the external EEPROM.

To generate the configuration file using the P9222-R/RN Windows GUI:

1. Place the receiver with the P9222-R/RN onto the WPC transmitter or apply 5V from an external power supply on the VRECT node.
2. Launch the P9222-R/RN GUI, go to the “Config” tab, click the “Rd EEPROM” button, and then click the “MODcap,INT,ID” button. A new popup window with the current values stored in the external EEPROM will be displayed.
3. Enter new values and click on the “Save cfg file” to generate a new configuration.

   The configuration can also be directly written to the external EEPROM by clicking the “Wr EEPROM” button. Note: The Write Protect function on the EEPROM must be disabled before writing to the EEPROM.

Figure 35. Modulation and INT Settings Tab



10. I2C Function

The P9222-R/RN uses the standard I²C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented by using 8 bits for data and 16 bits for addresses. The default slave address of the P9222-R/RN is 0x61h.

When writing to the P9222-R/RN, care should be taken to only write to registers marked exclusively as Read/Write (RW). Registers marked as Read Only (R) should never be sent a Write command or unexpected behavior may occur. In addition, register locations marked Reserved should not receive a Write command. When writing to a RW register that contains a combination of RW fields and reserved fields, a read-modify-write should be performed to the intended bit/field only. All other bits/field, including reserved bits/fields, should NOT be modified.

The P9222-R/RN Rx device operates in Rx mode. Depending on the firmware (FW) loaded into OTP memory or updated by the AP, the P9222-R/RN Rx will follow the programmed settings once connected wirelessly to a Tx. Some registers are defined and implemented for Read-only, some registers are Read/Write, and some registers are volatile and will be reset if power is cycled.

11. Registers

The P9222-R/RN uses the standard I²C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented using 8 bits for data and 16 bits for addresses. The default slave address of the P9222-R/RN is 0x61.

The following tables list address locations, field names, available operations (R or RW), default values, and functional descriptions of internally accessible registers contained within the P9222-R/RN. The OTP registers are loaded each time the device is powered and cannot be changed except by new firmware programmed into a blank device. The SRAM registers are available to make setting changes after the device is powered. These changes are reset to default when the power is cycled or the device is reset.

Table 11. Chip Part Number ID Register, Chip_ID_L (0x00), Chip_ID_H (0x01)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x00 [7:0]	Chip_ID_L	R	0x22	Chip ID low byte
0x01 [7:0]	Chip_ID_H	R	0x92	Chip ID high byte

Table 12. Chip Revision Register, Chip_Rev (0x02)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x02 [7:0]	Chip_Rev	R	0x02	Chip main revision. Latest chip revision is 0x02 (default).

Table 13. Status Registers, Status_L (0x34), Status_H (0x35)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x34 [7]	Reserved	R	0x0	Reserved
0x34 [6]	VRECTON	R	0x0	1 = Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. Interrupt event is generated on SET event. This bit can be used for turning on the charging indicator on the receiver.
0x34 [5]	TX Data Received	R	0x0	0 = Indicates no TX data is received. 1 = Indicates TX data is received and is ready to be read
0x34 [4]	Over voltage	R	0x0	0 = Indicates no such a condition exists. 1 = Indicates Over Voltage condition exists
0x34 [3]	Over current	R	0x0	0 = Indicates no such a condition exists 1 = Indicates Over Current condition exists
0x34 [2]	Over temperature	R	0x0	0 = Indicates no such a condition exists 1 = Indicates Over Temperature condition exists
0x34 [1:0]	Reserved	R	0x0	Reserved
0x35 [7:0]	Reserved	R	0x0	Reserved

Table 14. Interrupt Registers, INT_L (0x36), INT_H (0x37)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x36 [7]	Reserved	R	0x0	Reserved.
0x36 [6]	VRECTON_INT	R	0x0	AC power applied and stable interrupt.
0x36 [5]	TX Data Received	R	0x0	1 = Indicates a pending interrupt for TX Data Received. (No received data state change to data received state).
0x36 [4]	Over voltage	R	0x0	1 = Indicates a pending interrupt for Over voltage event
0x36 [3]	Over current	R	0x0	1 = Indicates a pending interrupt for Over current event
0x36 [2]	Over temperature	R	0x0	1 = Indicates a pending interrupt for Over temperature event
0x36 [1]	Reserved	R	0x0	Reserved
0x36 [0]	Mode_Changed	R	0x0	1 = Indicates a pending interrupt for mode or state change. For reading the current state, refer to Sys_Op_Mode (0x4C).
0x37 [7:0]	Reserved	R	0x00	Reserved

[a] If any bit in the two INT status registers is 1, and the corresponding bit in the two INT Enable registers is set to 1, /INT pad will be pulled down to indicate an interrupt event to AP.

Table 15. Interrupt Enable Registers, INT_Enable_L (0x38), INT_Enable_H (0x39)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x38 [6]	VRECTON_EN	R/W	0x1	AC power applied and stable interrupt enable.
0x38 [5]	TX Data Received	R/W	0x0	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [4]	Over voltage	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [3]	Over current	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [2]	Over temperature	R/W	0x1	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x38 [1]	Reserved	R	0x0	Reserved
0x38 [0]	Mode Changed	R/W	0x0	0 = Disable the interrupt. 1 = AP writes 1 to enable the interrupt from Interrupt Registers' corresponding bit.
0x39 [7:0]	Reserved	R	0x00	Reserved

Table 16. Interrupt Clear Registers, INT_Clear_L (0x3A), INT_Clear_H (0x3B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3A [6]	VRECTON_CLR	R/W	0x0	AC power applied and stable interrupt clear.
0x3A [5]	TX Data Received	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [4]	Over voltage	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [3]	Over current	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [2]	Over temperature	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3A [1]	Reserved	R	0x0	Reserved.
0x3A [0]	Stat_Mode_Changed	R/W	0x0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x3B [7:0]	Reserved	R	0x00	Reserved

Clearing all interrupts:

Clear all the interrupts that were generated using the INT_Clear_L (0x3A) and COM (0x4E) registers:

1. Write 0xFF to the INT_Clear_L (0x3A) register.
2. Write 0x20 to the COM (0x4E) register (set bit 5) to instruct the processor to clear the interrupt.

Clearing a single interrupt:

Clearing a single interrupt is a two-step process using the INT_Clear_L (0x3A) and COM (0x4E) registers:

1. In the INT_Clear_L (0x3A) register, set the bit that corresponds to the interrupt that will be cleared.
2. In the COM (0x4E) register, set bit 5 to instruct the processor to clear the interrupt.

   Note: Only the interrupt(s) that are selected with the INT_Clear_L (0x3A) register will be cleared.

Table 17. Vout Set Register, Vout_Set (0x3C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3C [7:0]	Vout_Set	R/W	0x32	Set the output voltage of the main LDO in 0.1V units. BPP default value: 0x32. Example: To set Vout to 5.5V, write 0d55 (0x37).

Table 18. ILIM Set Register, ILIM_Set (0x3D)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3D [7:0]	ILIM_Set[7:0]	R/W	0x0F	Main LDO output current limit (by which LDO will behave as a constant current source) set value. 100mA step, 0.1A-1.3A 0x00-0x0F: ILim = value * 0.1 (A)

Table 19. Battery Charge Status Register, CHG_Status (0x3E)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3E [7:0]	Charge status	R/W	0x00	A WPC charge status packet will be sent based on the following: 0x0 = Reserved 0x1 = Charge status packet sent with parameter = 1 (1%) 0x2 = Charge status packet send with parameter = 2 (2%) … 0x64 = Charge status packet send with parameter = 100 (100%) 0x65-0xFE = Reserved 0xFF = No battery charge device or not providing charge status packet

[a] After writing to this register, Send Charge Status bit of Command Register (0x4E) needs to be set for transmission to begin.

Table 20. End of Power Transfer Register, EPT (0x3F)[a]

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3F [7:0]	EPT/EOC/EOP Reason	R/W	0x00	A WPC End of Power Transfer packet/message will be sent based on the following: 0 = WPC mode, unknown EPT should be sent. 1 = WPC mode, End of Charge EPT packet should be sent. 2 = WPC mode, Internal Fault EPT packet should be sent. 3 = WPC mode, Over Temperature EPT packet should be sent. 4 = WPC mode, Over Voltage EPT packet should be sent. 5 = WPC mode, Over Current EPT packet should be sent. 6 = WPC mode, Battery Failure EPT packet should be sent. 7 = WPC mode, Reconfiguration EPT packet should be sent. 8 = WPC mode, No Response EPT packet should be sent. 9-254 = Reserved

[a] After writing to this register, the Send End of Power bit Command of Register (0x4E) must be set for transmission to begin.

Table 21. Vrect ADC Value Registers, ADC_Vrect_L (0x40), ADC_Vrect_H (0x41)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x40 [15:0]	ADC_Vrect [15:0]	R	0x0	Vrect ADC value in mV.

Table 22. Vout ADC Value Registers, ADC_Vout_L (0x42), ADC_Vout_H (0x43)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x42 [15:0]	ADC_Vout [15:0]	R	0x0	Vout ADC value in mV.

Table 23. Iout Value Registers, Iout_L (0x44), Iout_H (0x45)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x44 [15:0]	Iout [15:0]	R	0x0	Iout value in mA.

Table 24. Operating Frequency Registers, Op_Freq_L (0x48), Op_Freq_H (0x49) (RX Only)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x48 [15:0]	Op_Freq[7:0]	R	0x0	Operating frequency (AC signal frequency on the coil) in kHz.

Table 25. System Operating Mode Register, Sys_Op_Mode (0x4C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4C [7]	Reserved	R	0	Reserved.
0x4C [5]	Operational Mode	R	0x0	Indicates the FW is communicating to a Wireless Power Qi transmitter.
0x4C [4:1]	Reserved	R	0	Reserved.
0x4C [0]	LDOONMODE	R/W	0	Indicates output on VOUT.

Table 26. (AP to P9222-R/RN) Command Register, COM (0x4E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4E [7:6]	Reserved	R	0x0	Reserved.
0x4E [5]	Clear Interrupt	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 clears the interrupt corresponding to the bit(s) that have a value of 1 in Interrupt Clear Registers, and also sets the bit(s) in Interrupt Clear Registers to 0, as well as sets this bit to 0.
0x4E [4]	Send Charge Status	R/W	0x0	If the AP sets this bit to 1 then the P9222 the M0 sends the Charge Status packet (defined in the Battery Charge Status Register) to TX, and then sets this bit to 0 after execution.
0x4E [3]	Send End of Power	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 sends the End of Power packet (defined in the End of Power Transfer Register) to TX and then sets this bit to 0.
0x4E [2]	Reserved	R/W	0x0	Reserved.
0x4E [1]	Toggle LDO On/OFF	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 toggles LDO output once (from on to off, or from off to on), and then sets this bit to 0.
0x4E [0]	SEND RX Data	R/W	0x0	If the AP sets this bit to 1 then the P9222 M0 sends Data Command + Value to TX on Header and Payload of WPC Proprietary Packet, and then sets this bit to 0 after execution.

The P9222-R/RN will prioritize packets when sending commands and data to the Tx. Packets are prioritized as follows:

1. Received Power Packet (RPP)
2. Charge Status Packet (CSP)
3. Proprietary Packet (PPP)
4. Control Error Packet (CEP)

When using the AP to send CSP and PPP messages, care should be taken not to send them too frequently because they will delay the CEP transmission. It is not recommended to send CSP or PPP packets more than once every 250ms to avoid extended periods of time without allowing the P9222-R/RN to transmit a CEP.

Table 27. Outgoing Packet Header Register (0x50, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x50 [8:0]	PropOutPacket[0]	R/W	0x0	This register holds the header value of the outgoing packet

Table 28. Outgoing Packet Data Registers (0x51-0x57, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x51 [8:0]	PropOutPacket[1]	R/W	0x0	This register holds the first data value of the packet
0x52 [8:0]	PropOutPacket[2]	R/W	0x0	This register holds the second data value of the packet
0x53 [8:0]	PropOutPacket[3]	R/W	0x0	This register holds the third data value of the packet
0x54 [8:0]	PropOutPacket[4]	R/W	0x0	This register holds the fourth data value of the packet
0x55 [8:0]	PropOutPacket[5]	R/W	0x0	This register holds the fifth data value of the packet
0x56 [8:0]	PropOutPacket[6]	R/W	0x0	This register holds the sixth data value of the packet
0x57 [8:0]	PropOutPacket[7]	R/W	0x0	This register holds the seventh data value of the packet

Table 29. Incoming Packet Header Register (0x50, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x58 [8:0]	PropInPacket[0]	R/W	0x0	This register holds the header value of the incoming packet

Table 30. Incoming Packet Data Registers (0x59-0x5F, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x59 [8:0]	PropInPacket[1]	R/W	0x0	This register holds the first data value of the packet
0x5A [8:0]	PropInPacket[2]	R/W	0x0	This register holds the second data value of the packet
0x5B [8:0]	PropInPacket[3]	R/W	0x0	This register holds the third data value of the packet
0x5C [8:0]	PropInPacket[4]	R/W	0x0	This register holds the fourth data value of the packet
0x5D [8:0]	PropInPacket[5]	R/W	0x0	This register holds the fifth data value of the packet
0x5E [8:0]	PropInPacket[6]	R/W	0x0	This register holds the sixth data value of the packet
0x5F [8:0]	PropInPacket[7]	R/W	0x0	This register holds the seventh data value of the packet

Table 31. Die Temperature ADC Value Registers, ADC_Die_Temp_L (0x66), ADC_Die_Temp_H (0x67)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x66 [15:12]	Reserved	R	0x0	Reserved
0x66 [11:0]	ADC_Die_Temp_L	R	0x0	8 LSB of current Die Temperature ADC value. Formula converting ADC value to Die Temperature in Celsius Degree is: T_{DIE} = (DieTemp(adc) * 10/107) - 247

Table 32. Overvoltage Protection Set Register (0xB3, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB3 [7:3]	Reserved	R	0	Reserved.
0xB3 [2:0]	OV Set	R/W	0x02	Set Overvoltage Protection level. The hardware enables an additional DC Load when Vrect reaches 90% of the set level. The possible combinations are: 0x0 = 17V 0x1 = 20V 0x2 = 15V 0x3 = 13V 0x4-0x7 = 11V

Table 33. ASK Modulation Depth Register (0xB2, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB2 [7]	Reserved	R	0	Reserved.
0xB2 [6]	CM2EN	R/W	0x1	Enable CM2 pin to generate ASK modulation signal.
0xB2 [5]	CMBEN	R/W	0x0	Enable CMB pin to generate ASK modulation signal.
0xB2 [4]	CMAEN	R/W	0x0	Enable CMA pin to generate ASK modulation signal.
0xB2 [3]	CM1EN	R/W	0x1	Enable CM1 pin to generate ASK modulation signal
0xB2 [2:0]	Reserved	R	0	Reserved.

Table 34. Foreign Object Detection Registers, FOD (0x70-0x7E)[a]

The FOD registers are divided into eight pairs. Each pair has one byte for gain setting and one byte for offset setting. The first six pairs control the Received Power calculation for six power sectors during the Power Transfer phase. The seventh pair calibrates the internal DC Load. The set values of the FOD registers are found with the help of a Renesas developed calibration procedure using the nok9 tester.

The firmware initializes the FOD registers for BPP mode. The correct set is loaded at completion of the ID and Configuration Phase. The AP can modify the registers at any time if needed to update the values.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x70 [7:0]	GAIN_0	R/W	0xBC	FOD coefficients for Power Region 0: Gain (slope settings).
0x71 [7:0]	OFFSET_0	R/W	0x14	FOD coefficients for Power Region 0: Offset settings.
0x72 [7:0]	GAIN_1	R/W	0x98	FOD coefficients for Power Region 1: Gain (slope settings).
0x73 [7:0]	OFFSET_1	R/W	0x18	FOD coefficients for Power Region 1: Offset settings.
0x74 [7:0]	GAIN_2	R/W	0x9F	FOD coefficients for Power Region 2: Gain (slope settings).
0x75 [7:0]	OFFSET_2	R/W	0x0A	FOD coefficients for Power Region 2: Offset settings.
0x76 [7:0]	GAIN_3	R/W	0x94	FOD coefficients for Power Region 3: Gain (slope settings).
0x77 [7:0]	OFFSET_3	R/W	0x12	FOD coefficients for Power Region 3: Offset settings.
0x78 [7:0]	GAIN_4	R/W	0x97	FOD coefficients for Power Region 4: Gain (slope settings).
0x79 [7:0]	OFFSET_4	R/W	0x05	FOD coefficients for Power Region 4: Offset settings.
0x7A [7:0]	GAIN_5	R/W	0xA7	FOD coefficients for Power Region 5: Gain (slope settings).
0x7B [7:0]	OFFSET_5	R/W	0xCB	FOD coefficients for Power Region 5: Offset settings.
0x7C [7:0]	GAIN_6	R/W	0x14	FOD coefficients for Power Region 6: Gain (slope settings).
0x7D [7:0]	OFFSET_6	R/W	0x00	FOD coefficients for Power Region 6: Offset settings.
0x7E [7:0]	GAIN_7	R/W	0x01	FOD coefficients for Power Region 7: Gain (slope settings).
0x7F[7:0]	OFFSET_7	R/W	0x50	FOD coefficients for Power Region 7: Offset settings.

[a] These default FOD coefficients are calculated to PASS Nok9 CATS1 tester FOD tests using the P9222-R/RN reference design. FOD coefficients must be changed if the receiver design uses a different coil compared to the P9222-R/RN reference design, or if there is a large amount of friendly metal around the receiver coil.

Table 35. ADC Result Register (0xD4, 16-bit, OD2 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD4 [15:0]	AdcResult[0]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. By default it is configured to OD2. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: *AdcResult[0] * 2100 / 4096 = Voltage on OD2 in mV*

Table 36. ADC Result Register (0xD6, 16-bit, GP1 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD6 [15:0]	AdcResult[1]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. By default it is configured to GP1. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: *AdcResult[1] * 2100 / 4096 = Voltage on GP1 in mV*

Table 37. ADC Result Register (0xD8, 16-bit, GP2 in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xD8 [15:0]	AdcResult[2]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. The value is always in ADC counts and therefore must be converted to the desired units. For GPIOs the conversion is: *AdcResult[2] * 2100 / 4096 = Voltage on GP2 in mV*

Table 38. ADC Result Register (0xDA, 16-bit, Die Temperature in Default Config)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xDA [15:0]	AdcResult[3]	R	0	Configurable for GPIO, Temperature, Vout, Iout, or Vrect. The value is always in ADC counts and therefore must be converted to the desired units. For the conversion is: *AdcResult[3] * (2.1*200 / 4096) - 280 = Temperature in degC*

Table 39. External Thermistor Voltage on GP0 (0xB0, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xB0 [15:12]	Reserved	R	0	Reserved
0xB0 [11:0]	ExtTemp	R	0xFFF	12-bit raw data of the thermistor ADC reading on GP0 pin.

Table 40. VRECT Target Register (0x90, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x90 [15:0]	VrectTarget	R	0x4F3	Current value of VrectTarget in ADC codes. The ADC code to Voltage conversion formula is: Vrect(V) = Vrect(adc code) * 21(V) / 4095

Table 41. VRECT Knee Register (0x92, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x92 [7:0]	PwrKnee	R/W	0x0F	Threshold in units of 0.1W output power at which minimal window is applied.

Table 42. VRECT Correction Factor Register (0x93, 8-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x93 [7:0]	VrCorrFactor	R/W	0x19	Coefficient used in the Vrect Target calculation algorithm.

Table 43. VRECT Maximum Correction Register (0x94, 16-bit)

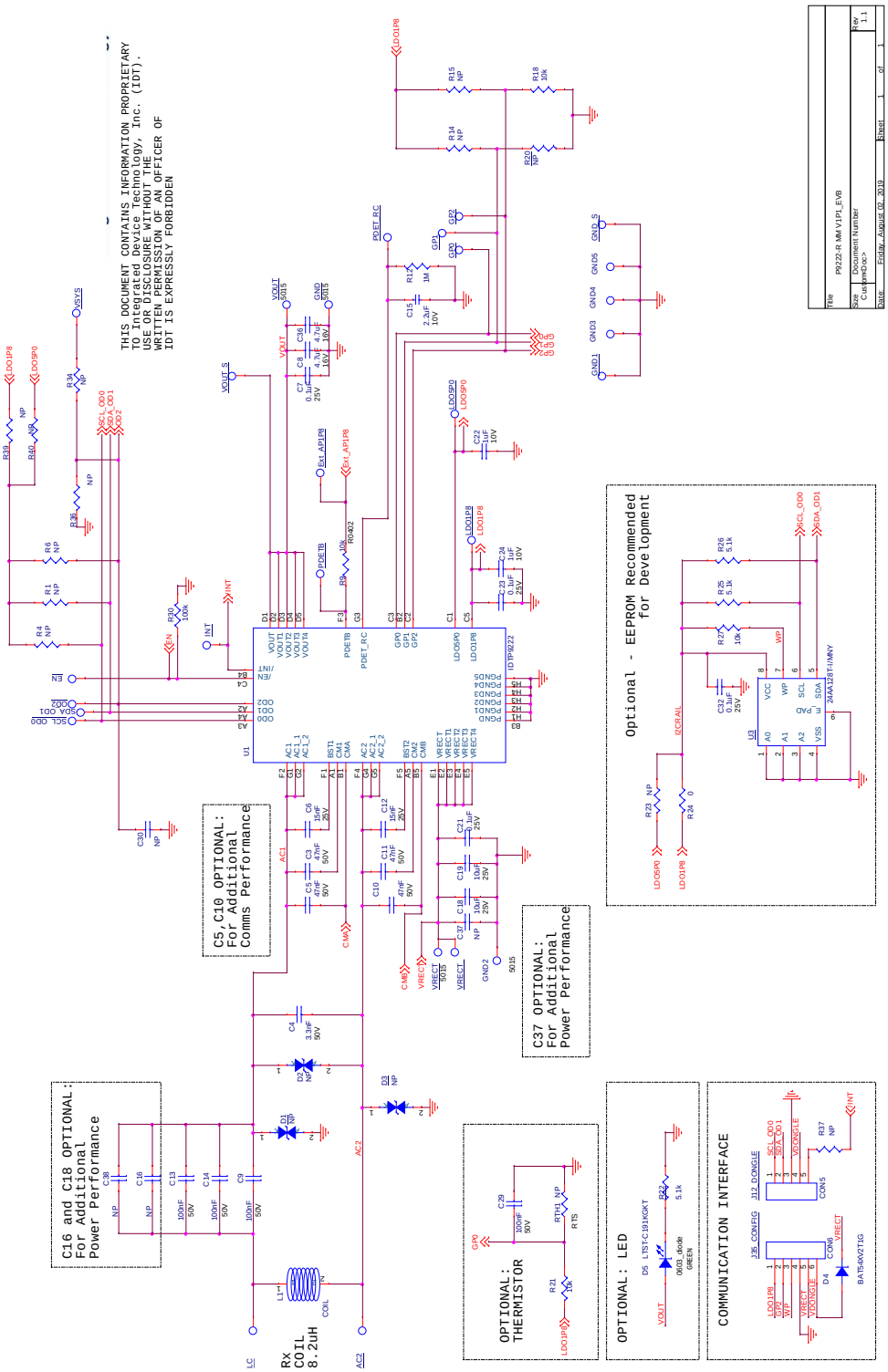
Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x94 [15:0]	VrMaxCorr	R/W	0xEA	Maximum width of the window in ADC codes.

Table 44. VRECT Minimum Correction Register (0x96, 16-bit)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x96 [15:0]	VrMinCorr	R/W	0x0D	Minimum width of the window in ADC codes.

12. Application Schematic

Figure 36. P9222-R/RN Application Schematic



13. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

14. Marking Diagram

- Line 1 is the manufacturer (Renesas).
- Line 2 is the truncated part number.
- Line 3: “YYWW” is the last digit of the year and week that the part was assembled. “**” denotes sequential lot number.
- Line 4: “$” denotes mark code; “R” is part of the device part number for P9222-R.
- Line 5: "NN” is the wafer number; “CC” is the column or X- coordinate of the wafer; “RR” is the row or Y-coordinate of the wafer

- Line 1 is the manufacturer (Renesas).
- Line 2 is the truncated part number.
- Line 3: “YYWW” is the last digit of the year and week that the part was assembled. “**” denotes sequential lot number.
- Line 4: “$” denotes mark code; “R” is part of the device part number for P9222-RN.
- Line 5: "NN” is the wafer number; “CC” is the column or X- coordinate of the wafer; “RR” is the row or Y-coordinate of the wafer

15. Ordering Information

Part Number[a]	Description	Package	MSL Rating	Carrier Type	Temperature Range
P9222-RAZGI8	Firmware factory programmed in internal OTP is WPC 1.2.4 Qi BPP compatible	40-WLCSP, 2.28 × 3.38 mm, 0.4mm pitch	MSL-1	Reel	-40°C to +85°C
P9222-RNAZGI8	Firmware factory programmed in internal OTP is WPC 1.3 Qi BPP compatible	40-WLCSP, 2.28 × 3.38 mm, 0.4mm pitch	MSL-1	Reel	-40°C to +85°C

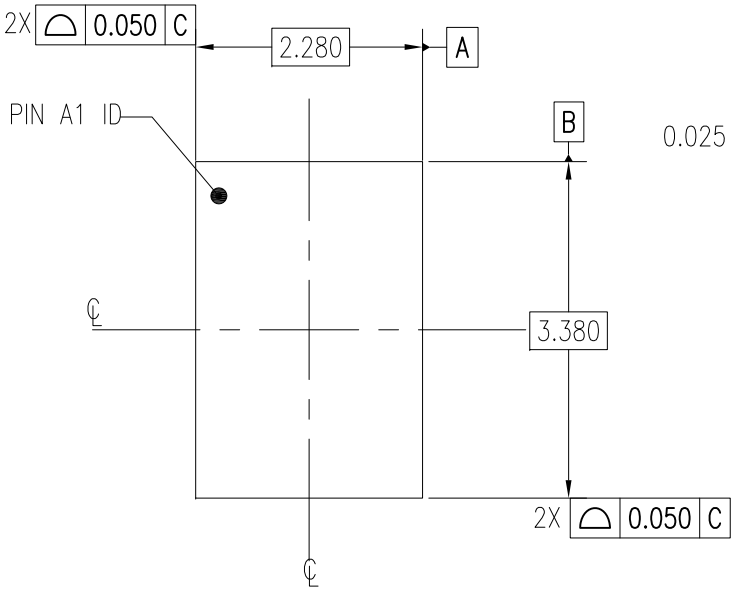
[a] In the part ordering number, the code after the dash indicates specific customer firmware requirements. A dash code of -0 indicates devices that have not been programmed.

16. Revision History

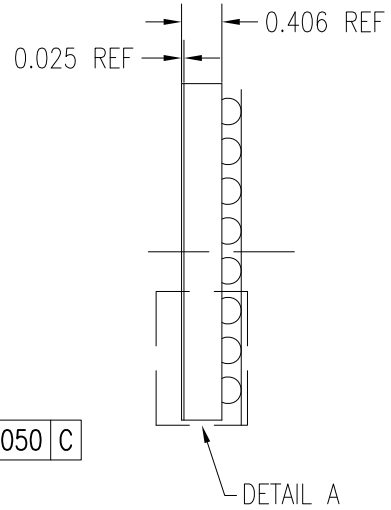
Revision Date	Description of Change
May 5, 2022	▪ Added P9222-RN part to the datasheet ▪ Completed other minor changes
September 8, 2021	▪ Added a new section, “Bi-directional User Data Communication” ▪ Completed other minor changes
September 27, 2019	Updated “Registers”.
September 5, 2019	Initial release.

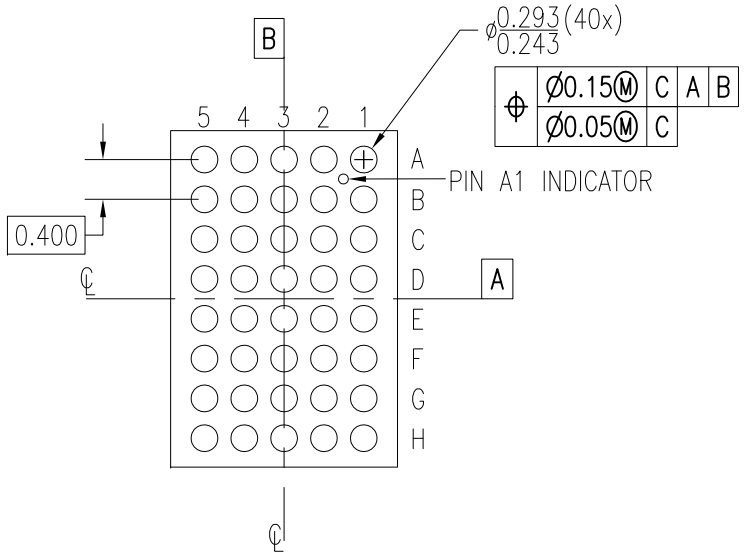
NOTES:
1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
11/15/16	00	INITIAL RELEASE	JH
12/14/17	01	ADD PIN 1 INDICATOR	JH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

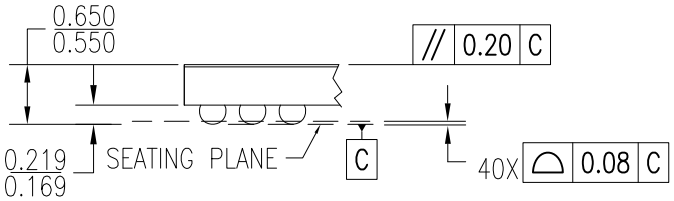


TOP VIEW





BOTTOM VIEW



DETAIL A
(ROTATED 90 DEG CW)

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± 0.05 ±
XXX± 0.012
XXXX±

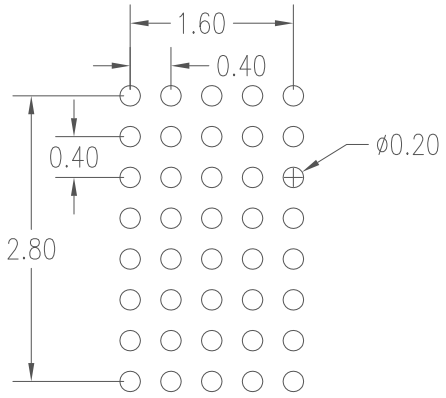
IDT™
www.IDT.com
6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE AZG40 Package Outline Drawing
2.280 x 3.380 x 0.60 mm Body
0.4mm Pitch DSBGA

SIZE	DRAWING No.	REV
C	PSC-4673	01

DO NOT SCALE DRAWING | SHEET 1 OF 2

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
11/15/16	00	INITIAL RELEASE	JH
12/14/17	01	ADD PIN 1 INDICATOR	JH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



RECOMMENDED LAND PATTERN DIMENSION

NOTE:
1. ALL DIMENSIONS ARE IN MM, ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEW ON PCB.
3. NSMD LAND PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION AS PER IPC-7351
   GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± 0.05 ±
XXX± 0.012
XXXX±

IDT™
www.IDT.com
6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE
AZG40 Package Outline Drawing
2.280 x 3.380 x 0.60 mm Body
0.4mm Pitch DSBGA

SIZE	DRAWING No.	REV
C	PSC-4673	01

DO NOT SCALE DRAWING

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2024 Renesas Electronics Corporation. All rights reserved.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

P9222-RAZGI8